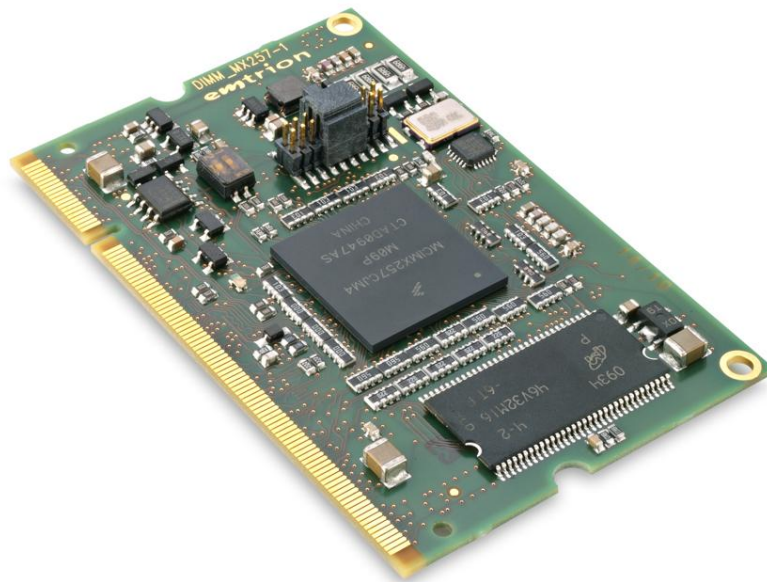


DIMM-MX257

Hardware Manual

Rev4 / 23.09.2011



© Copyright 2011 **emtrion GmbH**

All rights reserved. This documentation may not be photocopied or recorded on any electronic media without written approval. The information contained in this documentation is subject to change without prior notice. We assume no liability for erroneous information or its consequences. Trademarks used from other companies refer exclusively to the products of those companies.

Revision: **4 / 23.09.2011**

| Rev | Date/Signature | Changes |
|----------|----------------|--|
| 1 | 25.06.2010 | First revision |
| 2 | 28.06.2010 | Changed title from Hardware Description to Hardware Manual |
| 3 | 31.05.2011 | Added DDR SDRAM option 128MB (chapter 1, 2, 4.3, 4.22) Changed format of pin assignment tables (chapter 5) Added Note in I2C chapter (4.14) Added RTC chapter (4.16) Changed GPIO_A port (chapter 4.20) Added RGB table (chapter 4.8) Added IrDA (chapter 4.14) Added processor bus signal description (chapter 4.4) Added CSI signal description (chapter 4.10) |
| 4 | 23.09.2011 | Changed GPIO Port of red LED (chapter 4.21) Changed USB Host from to full speed (chapter 4.6) |

Contents

| | | |
|-------|-----------------------------------|----|
| 1 | Introduction..... | 5 |
| 2 | Block Diagram..... | 6 |
| 3 | Handling Precautions..... | 7 |
| 4 | Functional Description | 8 |
| 4.1 | Processor | 8 |
| 4.1.1 | Processor Clocks..... | 8 |
| 4.2 | NAND-Flash..... | 9 |
| 4.3 | RAM..... | 9 |
| 4.4 | Processor Bus..... | 9 |
| 4.5 | Ethernet..... | 10 |
| 4.6 | USB Host..... | 10 |
| 4.7 | USB Device | 11 |
| 4.8 | Graphic Display..... | 11 |
| 4.9 | Touch Interface..... | 11 |
| 4.10 | Video Input..... | 12 |
| 4.11 | Audio Interface, SSI port..... | 12 |
| 4.12 | SD-Card Interface..... | 12 |
| 4.13 | Serial Ports..... | 13 |
| 4.14 | IrDA | 13 |
| 4.15 | I ² C- Bus..... | 13 |
| 4.16 | RTC | 14 |
| 4.17 | SPI Interface | 14 |
| 4.18 | CAN | 14 |
| 4.19 | Analog Inputs..... | 14 |
| 4.20 | General Purpose I/Os..... | 15 |
| 4.21 | DIP Switches, Status LED | 15 |
| 4.22 | Memory Map | 16 |
| 4.23 | Interrupts | 16 |
| 4.24 | Reset | 16 |
| 4.25 | Debugging interface | 17 |
| 4.26 | Power Supply | 17 |
| 4.27 | DIMM Interface | 17 |
| 5 | Pin Assignments..... | 18 |
| 5.1 | J1, SODIMM..... | 18 |
| 5.2 | J2, Debugging Connector..... | 21 |
| 6 | Signal Characteristics | 22 |
| 6.1 | J1, SODIMM Connector..... | 22 |
| 6.2 | J2, Debugging Connector..... | 25 |
| 7 | Technical Characteristics | 26 |
| 7.1 | Electrical Specifications | 26 |
| 7.2 | Environmental Specifications..... | 26 |
| 7.3 | Mechanical Specifications | 26 |

| | | |
|-------|---------------------------|----|
| 7.3.1 | Dimensional Drawing | 27 |
| 81. | References | 28 |

1 Introduction

This document describes the functions of Board revision 2. The document revision 1 – 2 describes the functions of Board revision 1.

The DIMM-MX257 processor module is a SODIMM sized CPU board based on the i.MX processor i.MX257 from Freescale.

The processor core runs at 400 MHz and it includes a variety of functions required for multimedia or industry applications. These include LCD controller, camera interface, and sound input/output module.

The module includes a 256 MB NAND-Flash and 64 MB or 128MB of DDR SDRAM. In addition to the processor internal functions and the memory, a 10/100-Mbps Ethernet PHY is available.

All interfaces are accessible through the 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2,5V keying.

The power consumption of the whole board is less than 1,5W.

In the following table the features and interfaces of the DIMM-MX257 processor module are described.

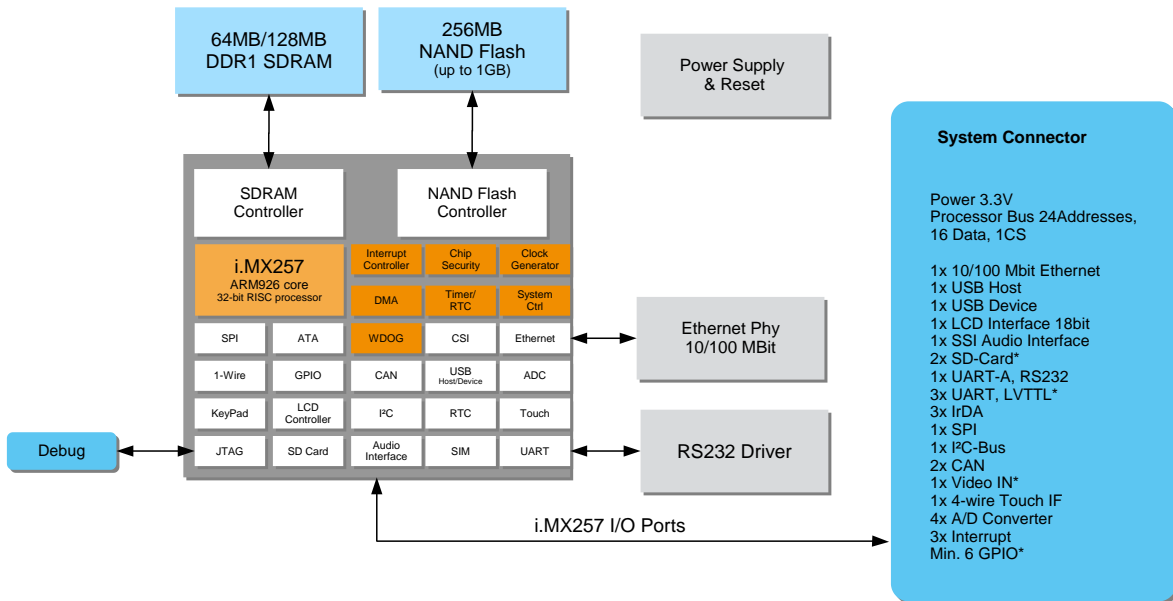
| DIMM-MX257 |
|--|
| 64MB or 128MB DDR SDRAM |
| 256MB NAND Flash |
| Processor Bus (16bit data, 24bit addresses, 1CS) |
| 1x 10/100Mbit Ethernet |
| 1x USB Host |
| 1x USB Device |
| 1x LCD Interface 16/18bit max. 800x600 Pixel |
| 1x 4 wire Touch |
| 1x SSI Audio |
| 1x UART RS232 |
| 1x SPI |
| 1x I2C |
| 2x CAN |
| 4x ADC |
| 3x IRQ |
| 1x/2x SD Card |
| 1x Video IN 8bit* |
| 2x/3x UART LVTTTL |
| 2x/3x IrDA |
| min. 2/6 GPIO |

*If the Video IN interface is used, the 2nd SD Card, the 3rd UART LVTTTL and GPIO's can't be used. Please contact emtrion GmbH for further details

The module is available in standard temperature range 0°C to 70°C and in the extended temperature range -40°C to 85°C.

2 Block Diagram

The following figure shows the block diagram of the DIMM-MX257.



*If the Video IN interface is used, the 2nd SD Card, the 3rd UART LVTTTL and some GPIO's can't be used. Please contact emtrion GmbH for further details

3 Handling Precautions

Please read the following notes prior to installing the DIMM-MX257 processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-MX257 does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The DIMM-MX257 processor board uses the i.MX processor i.MX257 from Freescale [1], a 32-bit RISC processor which runs at 400MHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides a lot of features such as:

- Interrupt controller
- Processor Bus Controller with SRAM, PSRAM and NOR Flash interface
- NAND Flash controller
- DDR SDRAM controller
- Four 32-bit timers
- 3/4 UARTs with 2x 32 byte FIFO
- 2/3 IrDA interfaces
- I2C bus interface
- SPI interface
- Video input module with camera capturing module and image processing unit*
- LCD Controller for TFT displays up to SVGA and 16/18 bpp
- 4 wire Touch controller
- Two CAN controllers
- Ethernet MAC 10/100Mbit
- Sound interface with I2S format
- USB 2.0 Host with full-speed mode
- 1/2 SD Card host controller
- 4-channel A/D converter
- JTAG debug interface

*If the Video IN interface is used, the 2nd SD Card, the 3rd UART LVTTTL and some GPIO's can't be used. Please contact emtrion GmbH for further details

Further details of the processor can be found in the i.MX257 hardware manual [1].

4.1.1 Processor Clocks

The 24MHz main clock is generated by a quartz crystal. This clock is multiplied by the internal PLL to 400 MHz and then divided by various software configurable dividers.

The following table shows the configured internal clocks:

| Clock | Frequency |
|------------------|-----------|
| CPU Clock | 400 MHz |
| Memory Clock | 133 MHz |
| Bus Clock | 66,66 MHz |
| SDRAM Clock | 133 MHz |
| Peripheral Clock | 66,66 MHz |

The RCLK clock input of the CPU is supplied by a 32,768 kHz clock from the RTC chip and it is used for date and time applications.

4.2 NAND-Flash

To store the operating system and application data, 256 MB NAND Flash are provided. A flash memory MT29F2G from Micron is used and connected to the eight bit NAND Flash controller of the processor.

To use the write protect function the WP# Pin of the Flash device is connected to the dedicated WP# pin of the NAND Flash controller of the processor. As default the signal is pulled down and the NAND Flash is protected.

For special applications, the NAND Flash size can be upgraded up to 1GB. (Please contact emtrion GmbH)

4.3 RAM

Two variants of the DIMM-MX257 are available. One with 64 MB DDR SDRAM and the other with 128MB DDR SDRAM The memory consists of one 512Mbit DDR SDRAM, (8M*16*4) or two 512Mbit DDR SDRAM (16M*8*4) and is connected to the SDRAM controller. They are clocked at 133 MHz and operated with CAS2.

As RAM device the MT46V32M16P-6 or MT46V64M8BN-6 from Micron is used.

The RAM is located in the address range 0x80000000 ... 0x83FFFFFF or 0x80000000 ... 0x87FFFFFF.

4.4 Processor Bus

The processor bus of the i.MX257 with 16bit data and 24bit addresses is routed to the SODIMM connector. The bus clock, the control signals and one chip select signal is also routed to the SODIMM connector. At this processor bus external devices or memory can be connected.

The processor bus signal level is 2,5V and the processor bus clock is 66,66MHz.

The address space is in the range 0xA0000000 ... 0xA0FFFFFF.

The following table describes the processor bus interface signals.

| Signals | Description |
|---------|---|
| A[23:0] | Address bus |
| D[15:0] | Data bus |
| CKIO | 66 MHz burst clock |
| WAIT# | Low active wait input signal (must not be used) |
| CS# | Low active chip select |
| RD# | Low active read signal |
| WE0# | Low active low byte D[7:0] selection signal |
| WE1# | Low active high byte D[15:8] selection signal |
| RD/WR# | Low active write enable signal |

4.5 Ethernet

The Ethernet interface is realized with the processor internal Media Access Controller (MAC) and an external Physical Layer Interface (PHY) LAN8720A from SMSC. The RMII interface is used for communication between the MAC and the PHY.

The Ethernet interface supports the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The registers of the Ethernet PHY can be configured via the Media Independent Interface (MII).

The Ethernet signals (ETH_TDP, ETH_TDM, ETH_RDP, ETH_RDM) as well as two status signals that serve to indicate the link status and the transfer speed are connected to the SODIMM connector. An appropriate 1:1 transformer must be added externally.

The signal LINK_LED# indicates if data packages are transferred. ("0" = traffic)

The signal SPEED_LED# indicates if the data is transferred with 100Mbit/s. ("0" = 100Mbit/s)

4.6 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the internal host controller of the i.MX257. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed and full-speed (12MHz).

To switch the bus power the control line USBH_PEN# is connected to the SODIMM connector. A logical "0" at the processor GPIO1-17 switches the power on, a logical "1" turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO2-22 ("0" = overcurrent).

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally. The data lines are internally terminated with 15-K Ω pulldown resistors.

4.7 USB Device

The USB device port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The interface is realized by the internal device controller of the i.MX257. The interface is USB 2.0 compliant, supporting data transfers at low-speed, full-speed (12MHz) and high-speed (480Mbps).

The data lines and the control line USBF_VBUS are available at the SODIMM connector. External 15-K Ω pulldown resistors are not required.

4.8 Graphic Display

The LCD controller of the i.MX257 can drive TFT displays with resolutions up to SVGA at 16/18bpp. The pixel clock for the display data is generated by an internal 64-bit pattern. Thus all timings can individually be adapted by software to the connected display.

All data and control lines are available at the SODIMM connector.

The following table shows the RGB colour mapping on the LCD_D[17:0] pins of the SODIMM connector.

| SODIMM LCD_D[17:0] | RGB565 (16bit) | RGB666 (18bit) |
|--------------------|----------------|----------------|
| LCD_D0 | - | B0 |
| LCD_D1 | B0 | B1 |
| LCD_D2 | B1 | B2 |
| LCD_D3 | B2 | B3 |
| LCD_D4 | B3 | B4 |
| LCD_D5 | B4 | B5 |
| LCD_D6 | G0 | G0 |
| LCD_D7 | G1 | G1 |
| LCD_D8 | G2 | G2 |
| LCD_D9 | G3 | G3 |
| LCD_D10 | G4 | G4 |
| LCD_D11 | G5 | G5 |
| LCD_D12 | - | R0 |
| LCD_D13 | R0 | R1 |
| LCD_D14 | R1 | R2 |
| LCD_D15 | R2 | R3 |
| LCD_D16 | R3 | R4 |
| LCD_D17 | R4 | R5 |

4.9 Touch Interface

A 4-wire touch interface is implemented via the processor internal touch controller. The pen interrupt is supported by that controller.

The touch interface signals (TOUCH_XP, TOUCH_XM, TOUCH_YP, TOUCH_YM) are available at the SODIMM connector.

If the touch interface is not used, these signals can be used as general purpose ADC input signals.

The touch interface can also be used as a 5-wire interface. In this case the analog input ANA_IN4 can be used as the wiper signal. Please contact emtrion GmbH for further details about this option.

4.10 Video Input

The i.MX257 has a video input unit (CSI) which can be used with different video sources, such as video codec or CMOS camera modules.

The interface at the DIMM-MX257 is realised with an 8-bit data-bus available at the SODIMM connector and supports various input formats.

The following table describes the CSI signals.

| Signals | Description |
|------------|--|
| CSI_D[7:0] | Video input data |
| CSI_CLK | Video input clock |
| CSI_HSYNC | Video input horizontal synchronization |
| CSI_VSYNC | Video input vertical synchronization |
| VIO_SRC | Video input source selection; "0" = CMOS camera (default); "1" = video codec |
| VIO_RST# | Video input source reset; "0" = reset; "1" = no reset (default) |

To switch between two video sources the signal VIO_SRC (GPIO3-17) is available. To reset the video codec on the base board the signal VIO_RST (GPIO2-21) can be used. Both signals are connected to the SODIMM connector

Attention:

If this interface is used, the 2nd SD Card, UART_D and GPIO_A to GPIO_D can't be used.

Please contact emtrion GmbH for further details about this option.

4.11 Audio Interface, SSI port

The i.MX257 processor has an integrated Audio module that can be used to send and receive audio data from external audio codecs.

The interface is connected to SODIMM connector, which allows the selection of an external audio codec. The processor can work in the SSI slave mode.

4.12 SD-Card Interface

The i.MX257 includes two SD Card interfaces to drive memory- or I/O cards. The signals are routed with all necessary pull up resistors to the SODIMM connector.

Attention:

The 2nd SD Card is only available if the Video IN interface is not used. Please contact emtrion GmbH for further details about this option.

4.13 Serial Ports

The DIMM-MX257 has up to four serial ports, depended on the module option. All serial ports are integrated in the processor i.MX257.

An overview of the UART interfaces is shown as follows:

| i.MX257 interface | SODIMM name | handshake signals |
|-------------------|-------------|-------------------|
| UART1 | UART_A | RTS, CTS |
| UART3 | UART_B | - |
| UART5* | UART_D | - |
| UART2 | UART_E | - |

*UART5 is only available if the Video IN interface is not used. Please contact emtrion GmbH for further details about this option.

UART_A has been implemented as a RS232 port. The signal lines of UART_B, UART_D and UART_E have LVTTTL level and will need to be configured by external drivers.

RS232 adaptors that can be plugged to a pin header are available from emtrion GmbH.

4.14 IrDA

Each UART port can also be used as low speed (115200bps) Infrared port (IrDA). So on the DIMM-MX257 there is the possibility of 3 IrDA ports. UART1 can't be used as IrDA port, because of the RS232 driver onboard. The UART RXD input signal is also the IrDA RXD input signal. The UART TXD output signal is also the IrDA TXD output signal.

4.15 I²C- Bus

The i.MX257 provides an I²C bus interface with transmission speeds up to 400 kb/s. The interface operates as a master.

One device is connected to the bus on DIMM-MX257:

| Slave | Device | Chip Address |
|-----------------|----------|--------------|
| Real Time Clock | DS1337U+ | 0x68 |

The bus connects to the SODIMM connector. The SCL and SDA lines are pulled up with 2,2kΩ resistors to 3,3V.

Note:

If the DIMM-MX257 module is used with an emtrion GmbH base board or with an emtrion GmbH display adapter some additional I²C addresses are reserved. Please contact emtrion GmbH for that reserved I²C addresses.

4.16 RTC

On the DIMM-MX257 there is a Real Time Clock (RTC). The RTC can be supplied with normal 3,3V or with an external coin cell, via the signal BAT. The RTC can be used for the clock time and the date. It can be configured via the I²C interface. The I²C chip address of the RTC is 0x68.

4.17 SPI Interface

The SPI interface of the i.MX257 processor is connected to the SODIMM connector. The four signals SPI_SCK, SPI_CS#, SPI_MOSI and SPI_MISO are routed to the SODIMM connector.

4.18 CAN

The i.MX257 includes two CAN controllers. The TX and RX signals are routed with all necessary pull up resistors to the SODIMM connector. For each CAN interface a CAN transceiver must be realized on the base board.

The signal level is 3,3V.

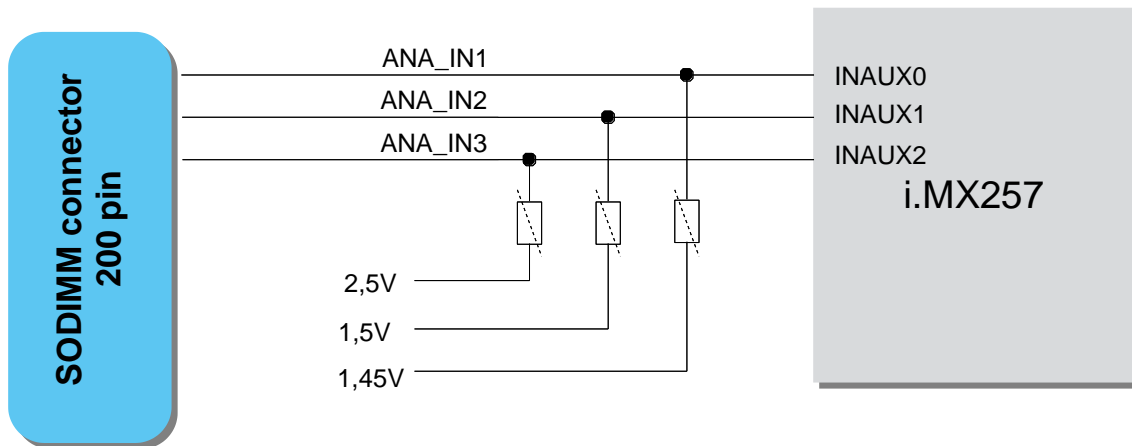
4.19 Analog Inputs

The i.MX257 contains a four channel A/D converter with a resolution of 12 bit. The maximum conversion time per channel is 8µs (125kHz).

The analog inputs have a permissible input voltage range of 0V ... 3,3V and connected directly to the SODIMM connector.

The analog inputs ANA_IN1, ANA_IN2 and ANA_IN3 can be used in different ways.

1. Normal analogue inputs (default)
2. Monitoring the onboard generated voltages 2,5V, 1,5V and 1,45V, via the on chip ADC.*
3. Monitoring the onboard generated voltages 2,5V, 1,5V and 1,45V, via an external ADC off board.*



*Please contact emtrion GmbH for that option.

4.20 General Purpose I/Os

Four port pins of the processor which can be used as GPIOs are routed to the SODIMM connector.

| SIGNAL | i.MX257 Port | Direction |
|---------|--------------|-----------|
| GPIO_A* | GPIO1-29 | In/Out |
| GPIO_B* | GPIO1-30 | In/Out |
| GPIO_C* | GPIO1-7 | In/Out |
| GPIO_D* | GPIO4-21 | In/Out |
| GPIO_E | GPIO1-26 | In/Out |
| GPIO_F | GPIO4-28 | In/Out |

*This GPIO is only available if the Video IN interface is not used. Please contact emtrion GmbH for further details about this option.

The port pin GPIO_E can be used as PWM output.

The signal level of each GPIO pin is 3,3V.

4.21 DIP Switches, Status LED

Two DIP switches are on the DIMM-MX257. Via that DIP switches the boot mode of the DIMM-MX257 module can be configured. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0. The following table describes the boot mode options.

| SW1 | SW2 | Boot Mode |
|-----|-----|------------------------|
| OFF | OFF | Internal Boot |
| OFF | ON | Reserved |
| ON | OFF | External (Direct) Boot |
| ON | ON | USB/UART Serial Boot |

Further details of the boot mode options can be found in the i.MX257 hardware manual [1].

A bicolour LED is connected to the port pins GPIO3-16 and GPIO3-19 of the i.MX257. If GPIO3-19 is high a green LED is lighting, if GPIO3-16 is high a red LED is lighting. If both ports are high both LEDs are on, which results in a yellow light.

4.22 Memory Map

In the following table the memory spaces of the external memory or devices is shown.

| Function | Bus Width | Address Region |
|-------------------|-----------|-------------------------|
| 64 MB DDR SDRAM* | 16-bit | 0x80000000 – 0x83FFFFFF |
| 128 MB DDR SDRAM* | 16-bit | 0x80000000 – 0x87FFFFFF |
| SODIMM | 8/16-bit | 0xA0000000 – 0xA0FFFFFF |

*Either 64MB DDR SDRAM or 128MB DDR SDRAM. Please contact emtrion GmbH. The timing characteristics of DDR SDRAM area is programmed according to the requirements of the DIMM-MX257 processor board.

The SODIMM area is reserved for external extensions and therefore configured with the slowest timing.

4.23 Interrupts

The processor i.MX257 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Each GPIO Input can be configured as an interrupt input. Eight dedicated interrupt input pins are available for external devices.

The use of the interrupt inputs is shown in the following table:

| GPIO Port | Source |
|-----------|---------------|
| GPIO3-15 | SODIMM (IRQ1) |
| GPIO2-31 | SODIMM (IRQ2) |
| GPIO3-0 | SODIMM (IRQ3) |
| GPIO4-3 | DS1337 |

The signal level of each interrupt is 3,3V.

4.24 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the 3,3V supply voltage of the board, the 1,45V Core voltage of the processor and the 2,5V DDR SDRAM voltage.
- Via the active low signal RESI# at the SODIMM connector
- Via the active low signal JTAG_RESI# at the Debug connector
- Via software by setting port pin HRESET_B (GPIO3-18) to 0 (only peripheral reset)

All resets are hardware resets of the whole board and issue a cold reset of the processor.

The duration of the reset signal is min. 140ms. For resetting external devices the reset signal is available as an output at the SODIMM connector.

4.25 Debugging interface

At the 20 pole header J2 all signals of the ARM9 debug interface and the Boot Mode signals are available.

Please contact emtrion GmbH for further details how to connect an emulator to J2.

4.26 Power Supply

A voltage of +3,3V, +/- 5%, @ max. 0.4 A must be supplied via the SODIMM connector. Further voltages for the processor and the other parts are generated on board.

4.27 DIMM Interface

All interface signals of the board and an SRAM like bus interface for external peripheral additions are available at the SODIMM connector which is named DIMM interface.

The DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2,5V keying. These sockets are available from various manufacturers.

Usage details of the connector and its electrical and mechanical characteristics can be found later in this document.

Notes:

The pin out of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pin out may damage the DIMM-MX257 and the carrier board.

Most of the pins are directly connected with the processor i.MX257n. For detailed electrical specification please refer to Section 3, Electrical Characteristics, in the i.MX257 datasheet [2]

5 Pin Assignments

5.1 J1, SODIMM

Type SODIMM, 200 pos, 2,5V keying

| Pin | Signal | Interface | | Signal | Pin |
|-----|------------|-----------|------------|-------------|----------|
| 1 | SPEED_LED# | Ethernet | USB Host | USBH_PEN# | 2 |
| 3 | ETH_TDP | | | USBH_OC# | 4 |
| 5 | ETH_TDM | | | USBH_DM | 6 |
| 7 | GND | | | USBH_DP | 8 |
| 9 | ETH_RDP | | USB Device | USBF_VBUS | 10 |
| 11 | ETH_RDM | | | USBF_DM | 12 |
| 13 | LINK_LED# | | | USBF_DP | 14 |
| 15 | n/c | Power | | GND | 16 |
| 17 | CAN1_TX | CAN | UART-A | UART1_TXD# | 18 |
| 19 | CAN1_RX | | | UART1_RXD# | 20 |
| 21 | UART2_TXD | UART-E | | UART1_RTS#* | 22 |
| 23 | UART2_RXD | | | UART1_CTS#* | 24 |
| 25 | UART5_TXD* | UART-D | | Touch | Touch_XP |
| 27 | UART5_RXD* | | Touch_XM | | 28 |
| 29 | n/c | UART-C | Touch_YP | | 30 |
| 31 | n/c | | Touch_YM | | 32 |
| 33 | UART3_TXD | UART-B | A/D | ANA_IN1 | 34 |
| 35 | UART3_RXD | | | ANA_IN2 | 36 |
| 37 | ANA_IN4 | A/D | | ANA_IN3 | 38 |
| 39 | +3V3 | Power | | GND | 40 |
| 41 | n/c | LCD | n/c | 42 | |
| 43 | n/c | | n/c | 44 | |
| 45 | n/c | | n/c | 46 | |
| 47 | LCD_D16 | | LCD_D17 | 48 | |
| 49 | LCD_D14 | | LCD_D15 | 50 | |
| 51 | LCD_D12 | | LCD_D13 | 52 | |

| | | | | | |
|------------|-----------|--------------|-------------|-----------|------------|
| 53 | LCD_D10 | | LCD_D11 | 54 | |
| 55 | LCD_D8 | | LCD_D9 | 56 | |
| 57 | LCD_D6 | | LCD_D7 | 58 | |
| 59 | LCD_D4 | | LCD_D5 | 60 | |
| 61 | LCD_D2 | | LCD_D3 | 62 | |
| 63 | LCD_D0 | | LCD_D1 | 64 | |
| 65 | +3V3 | Power | | GND | 66 |
| 67 | n/c | LCD | | n/c | 68 |
| 69 | LCD_DISP | | | LCD_DCK | 70 |
| 71 | LCD_HSYN | | | LCD_DON | 72 |
| 73 | LCD_VSYN | | | n/c | 74 |
| 75 | VOU_DEST | | | n/c | 76 |
| 77 | VOU_RST# | VIO | | VIO_D7* | 78 |
| 79 | n/c | | | VIO_D6* | 80 |
| 81 | VIO_CKO | | | VIO_D5* | 82 |
| 83 | VIO_CLK* | | | VIO_D4* | 84 |
| 85 | VIO_HD* | | | VIO_D3* | 86 |
| 87 | VIO_VD* | | | VIO_D2* | 88 |
| 89 | VIO_SRC | | | VIO_D1* | 90 |
| 91 | VIO_RST# | VIO_D0* | 92 | | |
| 93 | +3V3 | Power | | GND | 94 |
| 95 | SDC2_D0* | SDC2 | SDC1 | SDC1_D0 | 96 |
| 97 | SDC2_D1* | | | SDC1_D1 | 98 |
| 99 | SDC2_D2* | | | SDC1_D2 | 100 |
| 101 | SDC2_D3* | | | SDC1_D3 | 102 |
| 103 | SDC2_CMD* | | | SDC1_CMD | 104 |
| 105 | SDC2_CLK* | | | SDC1_CLK | 106 |
| 107 | SDC2_CD# | | | SDC1_CD# | 108 |
| 109 | SDC2_WP | SDC1_WP | 110 | | |
| 111 | SPI_SS# | SPI | | SPI_MISO | 112 |
| 113 | SPI_SCK | | | SPI_MOSI | 114 |

| | | | | | |
|------------|-----------|------------------------|--------------|------------|------------|
| 115 | SCL | I2C | Audio | AUDIO_BCK | 116 |
| 117 | SDA | | | AUDIO_LRC | 118 |
| 119 | SPDIF_IN | SPDIF | | AUDIO_DATI | 120 |
| 121 | SPDIF_OUT | | | AUDIO_DATO | 122 |
| 123 | GND | Power | | n/c | 124 |
| 125 | CAN2_RX | GPIO,TPU | CAN2_TX | 126 | |
| 127 | n/c | | GPIO_D* | 128 | |
| 129 | n/c | | GPIO_C* | 130 | |
| 131 | GPIO_F | | GPIO_B* | 132 | |
| 133 | GPIO_E | | GPIO_A* | 134 | |
| 135 | +3V3 | Power | GND | 136 | |
| 137 | A22 | Address A[23:0] | A23 | 138 | |
| 139 | A20 | | A21 | 140 | |
| 141 | A18 | | A19 | 142 | |
| 143 | A16 | | A17 | 144 | |
| 145 | A14 | | A15 | 146 | |
| 147 | A12 | | A13 | 148 | |
| 149 | A10 | | A11 | 150 | |
| 151 | A8 | | A9 | 152 | |
| 153 | A6 | | A7 | 154 | |
| 155 | A4 | | A5 | 156 | |
| 157 | A2 | | A3 | 158 | |
| 159 | A0 | | A1 | 160 | |
| 161 | +3V3 | Power | GND | 162 | |
| 163 | D14 | Data D[15:0] | D15 | 164 | |
| 165 | D12 | | D13 | 166 | |
| 167 | D10 | | D11 | 168 | |
| 169 | D8 | | D9 | 170 | |
| 171 | D6 | | D7 | 172 | |
| 173 | D4 | | D5 | 174 | |
| 175 | D2 | | D3 | 176 | |

| | | | | | |
|------------|--------|--------------------|--------------|------------|------------|
| 177 | D0 | Bus Control | D1 | 178 | |
| 179 | CKIO | | n/c | 180 | |
| 181 | n/c | | n/c | 182 | |
| 183 | RD# | | IRQ1# | 184 | |
| 185 | RD/WR# | | IRQ2# | 186 | |
| 187 | WE0# | | IRQ3# | 188 | |
| 189 | WE1# | | RESO# | 190 | |
| 191 | n/c | | RESI# | 192 | |
| 193 | n/c | | n/c | 194 | |
| 195 | WAIT# | | n/c | 196 | |
| 197 | CS# | | n/c | 198 | |
| 199 | BAT | | Power | GND | 200 |

*Either This GPIO, UART and SDC2 signals or the Video IN interface are available. Please contact emtrion GmbH for further details about this option.

5.2 J2, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

| Pin | Signal | Pin | Signal |
|-----------|------------|-----------|-------------|
| 1 | RTCK | 2 | TCK |
| 3 | GND | 4 | GND |
| 5 | +3V3 | 6 | TRST# |
| 7 | +3V3 | 8 | +3V3 |
| 9 | n/c | 10 | TDO |
| 11 | BOOT_MODE1 | 12 | JTAG_DE# |
| 13 | BOOT_MODE0 | 14 | TMS |
| 15 | JTAG_MODE | 16 | TDI |
| 17 | GND | 18 | DBG_ACK |
| 19 | JTAG_RESI# | 20 | JTAG_RESET# |

6 Signal Characteristics

Abbreviations:

AI analogue input
 AO analogue output
 A I/O analogue bidirectional
 I digital input
 O digital output
 I/O digital bidirectional

PU xK x K Ω pullup resistor
 PD xK x K Ω pulldown resistor
 SR xR x Ω series resistor
 IPU xK processor internal x K Ω pullup resistor
 IPD xK transistor internal x K Ω pulldown resistor

6.1 J1, SODIMM Connector

| Name | Direction | Add. Wiring | Volt [V] | Description |
|-------------------|-----------|---------------------|----------|-------------------------|
| Ethernet | | | | |
| SPEED_LED# | O | - | 3,3 | 100 Mbit indicator |
| SPEED_LED# | O | - | 3,3 | 100 Mbit indicator |
| ETH_TDP | AO | - | - | TX diff. output pos. |
| ETH_TDM | AO | - | - | TX diff. output neg. |
| ETH_RDP | AI | - | - | RX diff. input pos. |
| ETH_RDN | AI | - | - | RX diff. input neg. |
| LINK_LED# | O | - | 3,3 | traffic indicator |
| USB Host | | | | |
| USBH_PEN# | O | PU 100K IPU 100K | 3,3 | Power enable for switch |
| USBH_OC# | I | PU 100K IPU 100K | 3,3 | Overcurrent from switch |
| USBH_DP | I/O | SR 33 | 3,3 | Diff. data positive |
| USBH_DM | I/O | SR 33 | 3,3 | Diff. data negative |
| USB Device | | | | |
| USBF_VBUS | I | - | 5 | VBUS detection |
| USBF_DP | I/O | - | 3,3 | Diff. data positive |
| USBF_DM | I/O | - | 3,3 | Diff. data negative |
| UART | | | | |
| UART1_TXD# | O | IPU 100K | RS232 | RS232 transmit data |
| UART1_RXD# | I | IPU 100K | RS232 | RS232 receive data |
| UART1_RTS# | O | IPU 100K | RS232 | RS232 modem control |
| UART1_CTS# | I | IPU 100K | RS232 | RS232 modem control |
| UART2_TXD# | O | IPU 100K | 3,3 | transmit data |
| UART2_RXD# | I | IPU 100K | 3,3 | receive data |
| UART3_TXD# | O | IPU 100K | 3,3 | transmit data |
| UART3_RXD# | I | IPU 100K | 3,3 | receive data |

| | | | | |
|---|-------|--------------------|-----|---|
| UART5_TXD# | O | IPU 100K | 3,3 | transmit data |
| UART5_RXD# | I | IPU 100K | 3,3 | receive data |
| CAN | | | | |
| CAN1_TX | O | PU 10K IPU 100K | 3,3 | transmit data |
| CAN1_RX | I | PU 10K IPU 100K | 3,3 | receive data |
| CAN2_TX | O | PU 10K IPU 100K | 3,3 | transmit data |
| CAN2_RX | I | PU 10K IPU 100K | 3,3 | receive data |
| 4-Wire Resistive Touch Interface | | | | |
| TOUCH_XP | A I/O | - | 3,3 | X plus terminal |
| TOUCH_XM | A I/O | - | 3,3 | X minus terminal |
| TOUCH_YP | A I/O | - | 3,3 | Y plus terminal |
| TOUCH_YM | A I/O | - | 3,3 | Y minus terminal |
| Analog Input | | | | |
| ANA_IN1 | A I/O | - | 3,3 | 12 bit analog input |
| ANA_IN2 | A I/O | - | 3,3 | 12 bit analog input |
| ANA_IN3 | A I/O | - | 3,3 | 12 bit analog input |
| ANA_IN4 | A I/O | - | 3,3 | 12 bit analog input |
| LCD (Graphic Display) | | | | |
| LCD_DON | O | - | 3,3 | LCD display enable signal |
| LCD_DISP | O | PD 10K | 3,3 | LCD data enable signal |
| LCD_VSYNC | O | PD 10K | 3,3 | LCD frame sync output |
| LCD_HSYNC | O | PD 10K | 3,3 | LCD line sync output |
| LCD_D[17:16] | O | IPU 100K | 3,3 | LCD colour data |
| LCD_D[15, 13, 12, 10: 5, 2, 1] | O | PD 10K | 3,3 | LCD colour data |
| LCD_D[14, 11, 4, 3, 0] | O | PU 10K | 3,3 | LCD colour data |
| LCD_DCK | O | PD 10K | 3,3 | LCD data clock |
| VIO (Video Input Unit)* | | | | |
| VIO_D[7:0] | I | IPU 100K | 3,3 | Video image input data |
| VIO_CLK | I | IPU 47K | 3,3 | Video clock input |
| VIO_HD | I | IPU 47K | 3,3 | Video hsync input |
| VIO_VD | I | IPU 47K | 3,3 | Video vsync input |
| VIO_CKO | O | IPU 47K | 3,3 | Clock output |
| VIO_SRC | O | IPU 100K | 3,3 | Selection of either camera or video codec input |
| VIO_RST# | O | IPU 100K | 3,3 | Reset signal for video device |
| SPI | | | | |
| SPI_CS# | O | IPU 100K | 3,3 | Chip select output |
| SPI_SCK | O | IPU 100K | 3,3 | Clock output |
| SPI_MISO | I | IPU 100K | 3,3 | Input data from slave |
| SPI_MOSI | O | IPU 100K | 3,3 | Output data to slave |
| SD Card Interface | | | | |
| SDC1_D[3:0] | I/O | IPU 47K | 3,3 | SDC data |
| SDC1_CMD | I/O | IPU 47K | 3,3 | CMD signal |
| SDC1_CLK | O | IPU 47K | 3,3 | SDC Clock output |

| | | | | |
|----------------------|-----|----------|-----------|--------------------------------|
| SDC1_CD# | I | PU 100K | 2,5 | Card detect input |
| SDC1_WP | I | PU 100K | 2,5 | Write protect input |
| SDC2_D[3:0] | I/O | IPU 47K | 3,3 | SDC data |
| SDC2_CMD | I/O | IPU 47K | 3,3 | CMD signal |
| SDC2_CLK | O | IPU 47K | 3,3 | SDC Clock output |
| SDC2_CD# | I | PU 100K | 2,5 | Card detect input |
| | | IPU 100K | | |
| SDC2_WP | I | PU 100K | 2,5 | Write protect input |
| | | IPU 100K | | |
| I2C | | | | |
| SCL | I/O | PU 2K2 | 3,3 | I ² C clock signal |
| | | IPU 100K | | |
| SDA | I/O | PU 2K2 | 3,3 | I ² C data signal |
| | | IPU 100K | | |
| Audio | | | | |
| AUDIO_BCK | I/O | IPU 100K | 3,3 | Sound bit clock |
| AUDIO_LRC | I | IPU 100K | 3,3 | Sound L/R signal |
| AUDIO_DATI | I | IPU 100K | 3,3 | Sound serial input data |
| AUDIO_DATO | O | IPU 100K | 3,3 | Sound serial output data |
| General Purpose I/O | | | | |
| GPIO[A:D, F] | I/O | IPU 100K | 3,3 | digital input / output |
| GPIO_E | I/O | PD 10K | 3,3 | digital input / output |
| Bus Interface | | | | |
| A[23:0] | O | SR 56R | 2,5 | Processor address bus |
| D[15:0] | I/O | SR 39R | 3,3 | Processor data bus |
| | | IPU 100K | | |
| CKIO | O | SR 47R | 2,5 | 66 MHz bus clock |
| WAIT# | I | PU 10K | 3,3 | Wait Input |
| | | IPU 100K | | |
| CS# | O | PU 10k | 2,5 | Chip select output |
| | | SR 56R | | |
| RD# | O | SR 56R | 2,5 | Read signal |
| WE0# | O | SR 56R | 2,5 | Write access on even address |
| WE1# | O | SR 56R | 2,5 | Write access on odd address |
| RD/WR# | O | SR 56R | 2,5 | Data direction signal |
| IRQ1 | I | PU 10K | 3,3 | Interrupt input |
| | | IPU 100K | | |
| IRQ2 | I | PU 10K | 3,3 | Interrupt input |
| | | IPU 100K | | |
| IRQ3 | I | PU 10K | 3,3 | Interrupt input |
| | | IPU 100K | | |
| RESI# | I | PU 10K | 3,3 | Reset input from carrier board |
| RESO# | O | - | 3,3 | Reset output to carrier board |
| BAT | - | - | 1,8 – 3,0 | Battery backup input for RTC |
| +3V3 | - | - | - | + 3,3V supply |
| GND | - | - | - | Ground |

*If the Video IN interface is used, the 2nd SD Card, the 3rd UART LVTTTL and GPIO's can't be used.
Please contact emtrion GmbH for further details

6.2 J2, Debugging Connector

| Name | Direction | Add. Wiring | Volt [V] | Description |
|------------------------|-----------|----------------------------|----------|------------------------|
| Debug Interface | | | | |
| TCK | I | PD 10K IPD 100K | 3,3 | JTAG clock input |
| TMS | I | PU 10K | 3,3 | JTAG mode select input |
| TRST# | I | PD 10K IPU 47K | 3,3 | H-UDI reset input |
| TDI | I | PU 10K IPU 47K | 3,3 | Data input |
| TDO | O | SR 33 PU 10K IPU 47K | 3,3 | Data output |
| RTCK | O | PD 10K | 3,3 | return TCK |
| JTAG_MODE | I | PD 10K IPU 100K | 3,3 | |
| JTAG_DE# | I | PU 10K IPU 47K | 3,3 | |
| DBG_ACK | O | PD 10K | 3,3 | |
| Miscellaneous | | | | |
| JTAG_RESET# | I | PU 100K | 3,3 | Debugger Reset input |
| JTAG_RESI# | I | PU 10K | 3,3 | Manual Reset input |
| BOOT_MODE0 | I | PD 10K IPD 100K | 3,3 | Boot mode selection |
| BOOT_MODE1 | I | PD 10K IPD 100K | 3,3 | Boot mode selection |
| +3V3 | - | - | - | + 3,3V supply |
| GND | - | - | - | Ground |

7 Technical Characteristics

7.1 Electrical Specifications

| | |
|----------------------------|--------------|
| Supply voltage | 3,3 V, +/-5% |
| Current consumption | 0.4 A max. |

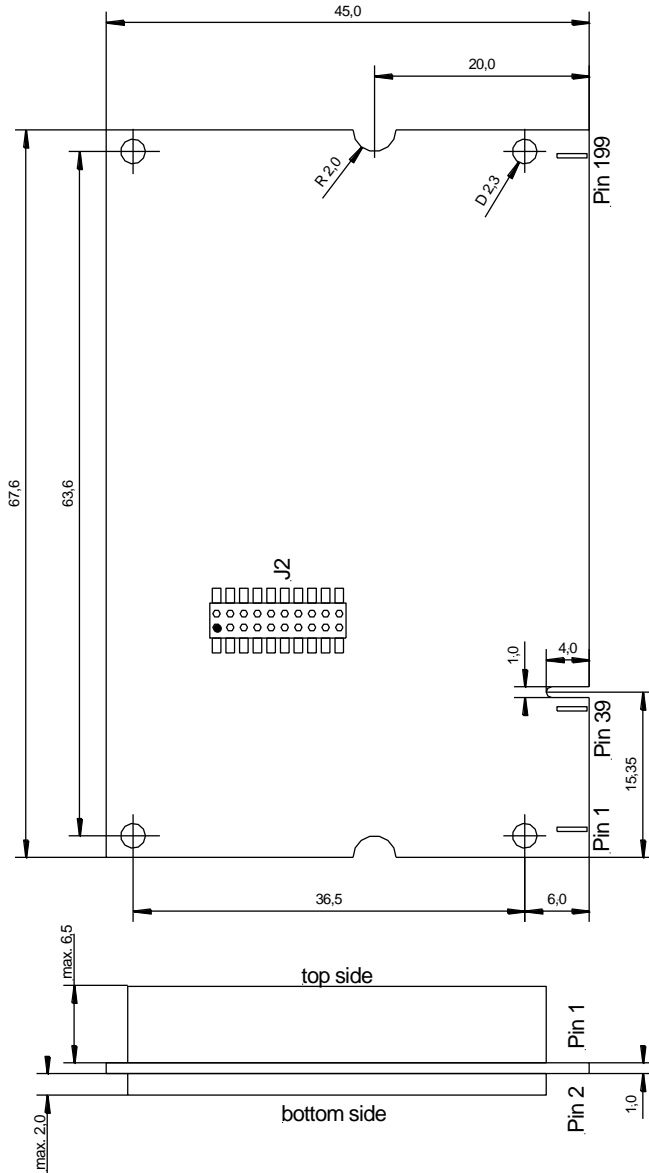
7.2 Environmental Specifications

| | |
|------------------------------|----------------------------|
| Operating temperature | |
| Standard: | 0 ... +70°C |
| Extended: | -40 ... +85°C |
| Storage temperature | -40 ... +125°C |
| Relative humidity | 0 ... 95 %, non-condensing |

7.3 Mechanical Specifications

| | |
|-------------------|-------------------------------------|
| Weight | approx. 16 g |
| Board | Glasepoxi FR-4, UL-listed, 8 layers |
| Dimensions | 67.6 mm x 45.0 mm x 10.0 mm |

7.3.1 Dimensional Drawing



8 1. References

- [1] i.MX257
Hardware Manual
i.MX25 Multimedia Applications Processor Reference Manual
Rev. 2, 01/2011
Freescale semiconductor

- [2] i.MX257
Datasheet
i.MX25 Applications Processor for Consumer and Industrial Products
Rev. 8, 01/2011
Freescale semiconductor