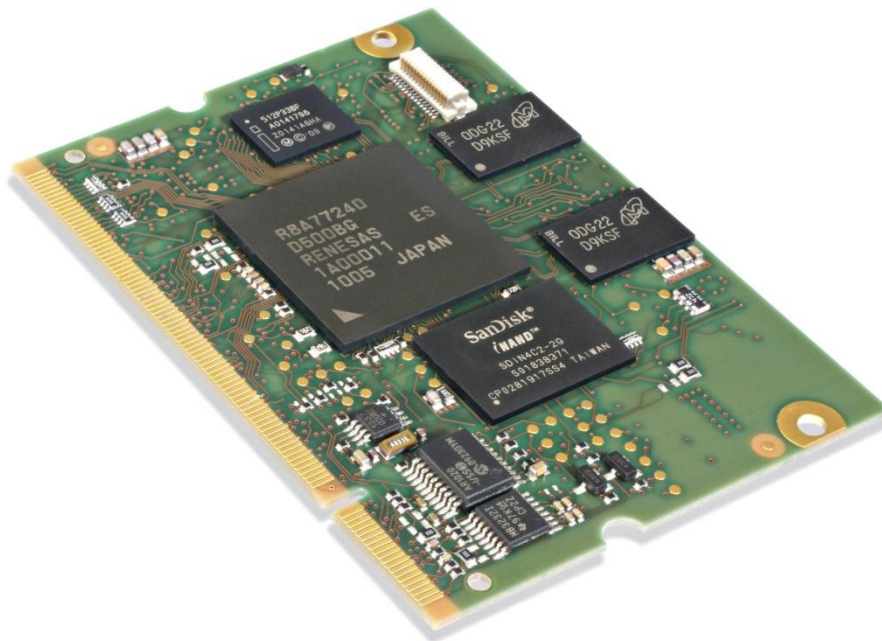


DIMM-SH7724

Processor Module with SH7724

Hardware Description

Rev3 / 11.08.2011



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1	31.01.2011/Sr	First revision
2	04.04.2011/Sr	- Chapter "NAND-Flash": Device information removed - Chapter "Graphic Display": Default assembly of the LCDLCLK series resistor R22 changed.
3	11.08.2011/Sr	- Block Diagram updated - Chapter "NOR-Flash" updated. - Chapter "Pin Assignment - SODIMM Connector": LCD_LCLK corrected

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1 Introduction

The DIMM-SH7724 processor module is a SODIMM sized CPU board based on the SuperH SH4A processor SH7724 from Renesas.

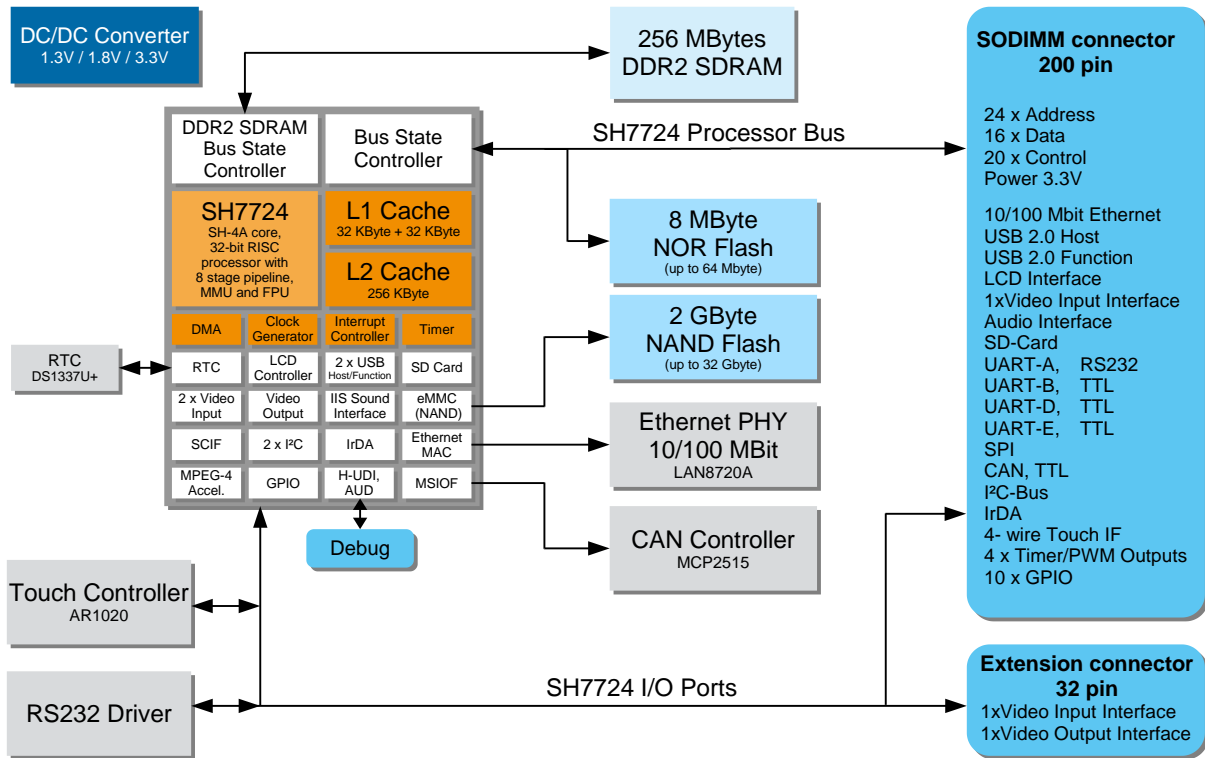
The processor core runs at 500 MHz and it includes a variety of functions required for multimedia applications. These include MPEG4 and H.264 accelerators, a 2D graphics accelerator, LCD controller, two camera interfaces and a sound input/output module.

The standard module comes with up to 64 MByte NOR-Flash, up to 32 GByte NAND-Flash and 256 MByte of DDR2 SDRAM. The CPU has an internal Ethernet MAC and two USB Controllers, which are used as USB Host and USB Device. Additionally a CAN controller and a touch controller are available.

All interfaces are accessible through the 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2.5 V keying.

The power consumption of the whole board is about 1W.

2 Block Diagram



3 Handling Precautions

Please read the following notes prior to installing the DIMM-SH7724 processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-SH7724 does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The DIMM-SH7724 processor board uses the SuperH SH4A processor SH7724 from Renesas [1], a 32 bit RISC processor which runs at 500 MHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides a lot of features such as:

- Floating-point unit
- Memory management unit
- Cache memory, 32 kByte instruction and 32 kByte data cache, 256 kByte L2 cache
- Interrupt controller with 15 levels and nine external interrupt pins
- Bus state controller with SRAM, Burst ROM, SDRAM and PCMCIA interface
- DDR2 SDRAM controller
- 12-channel DMA controller with two external inputs
- Six 32 bit auto-reload timers
- Four 16 bit timer with TTL output (e.g. for PWM)
- 32 bit compare match timer
- Watchdog timer
- Real time clock
- Three UARTs with 16 byte FIFO and high speed mode
- Three UARTs with 64 byte FIFO and high speed mode
- Two I²C bus interfaces
- Two SPI interfaces
- Two Video input modules with camera capturing module and image processing unit
- Video output unit, digital outputs conform to ITU-R BT.601, ITU-R BT.656
- Video processing unit for MPEG-4 H.264 encoding and decoding
- LCD Controller for TFT displays up to SXGA and 24 bpp
- 2D graphic accelerator
- JPEG processing unit
- Sound interface with PCM and I2S format with two internal audio DSPs
- Ethernet controller MAC, 10/100Mbit
- Two USB 2.0 Controller with high-speed mode, which can be used for Host or Device
- SD Card host controller
- MMC interface, booting from eMMC NAND-Flash supported
- H-UDI debug interface

Further details of the processor can be found in the SH7724 hardware manual [1].

4.1.1 Processor Clocks

The RCLK clock input of the CPU is supplied by a 32,768 kHz clock from the RTC chip and used as main clock. This clock is multiplied by the internal PLL to 500 MHz and then divided by various software configurable dividers.

The following table shows the configured internal clocks:

Clock	Frequency
CPU Clock ($I\phi$)	500 MHz
Memory Clock ($U\phi$)	166,6 MHz
SH Clock ($SH\phi$)	166,6 MHz
Bus Clock ($B\phi$)	83,3 MHz
M1 Clock ($M1\phi$)	83,3 MHz
Peripheral Clock ($P\phi$)	41,6 MHz

4.1.2 Boot Mode

The SH7724 can boot from the NOR-Flash via the bus state controller area 0 or from the NAND-Flash controller. The boot mode is configured with 10K pull-up or pull-down resistors at the BOOT pin of the SH7724.

BOOT pin	Boot source	R38 fitted	R39 fitted
0	NOR-Flash	NO	YES
1	NAND-Flash	YES	NO

4.2 Flash

4.2.1 NAND-Flash

As non-volatile memory an eMMC NAND-Flash is used. An eMMC combines a NAND-Flash device and a NAND-Flash controller in one package and can be addressed like memory cards with the MMC protocol. The Multi Media Card Interface (MMCIF) of the SH7724 supports booting from eMMC devices with a capacity up to 32 GByte.

4.2.2 NOR-Flash

To store Bootloader and special firmware a 8 MByte NOR-Flash PC28F640P33 [2] from Numonyx is provided and connected to the 16-bit wide data bus. Optionally NOR-Flash with up to 64 MByte can be used.

To use the write protect function the WP# Pin of the Flash device is connected to the processor GPIO PTB4. As default the signal is pulled down and the NOR Flash is protected.

Also the VPP pin of the NOR-Flash can be controlled by a processor GPIO. This improves the write protection function. The VPP pin is connected via an inverter to the GPIO PTB5. As default the GPIO pin is pulled up.

The following table shows the protection mode according to the GPIO pin states of the CPU:

PTB4 [WP#]	PTB5 [VPP#]	write protection
0	0	Only locked blocks are write protected
0	1	All blocks write protected
1	0	No write protection
1	1	All blocks write protected

For further information to the write protection, please see the datasheet of the NOR-Flash [2].

The flash device is located in area 0 from 0x00000000 ... 0x007FFFFF.

There is also the option to remove the NOR-Flash and booting only from NAND-Flash. Please ask emtrion for variants without NOR-Flash.

4.3 SDRAM

256 MByte DDR2 SDRAM are available as main memory. The memory consists of two 1024 MBit DDR2 SDRAMs, type 8M*16*8, that are connected in parallel to a 32-bit wide data bus. They are clocked at 166,6 MHz and operate with CAS3.

As SDRAM devices two MT47H64M16HR-3 from Micron are used.

The RAM is located in area 2, 3, 4 and 5, in the address range 0x08000000 ... 0x17FFFFFFF.

4.4 Ethernet Controller

The SH7724 processor has an internal Ethernet Media Access Controller (MAC). Additionally the Ethernet PHY LAN8720A from SMSC is connected via the RMII interface to the internal MAC of the CPU.

Supported are 10/100 MBit transfers, auto-MDIX and auto-negotiation.

The Ethernet signal lines as well as two status signals that serve to indicate the link status and the transfer speed are connected to the SODIMM connector. An appropriate 1:1 transformer, which center tap is sourced by 3.3V, must be added externally.

4.5 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the first internal host controller of the SH7724. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed-, full-speed and high-speed.

To switch the bus power, the control line USBH_PEN# is connected to the SODIMM connector. A logical "0" at the processor GPIO PTB3 switches the power on; a logical "1" turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO PTB2 ("0" = overcurrent).

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally. The data lines are internally terminated with 15-K Ω pulldown resistors.

4.6 USB Function

The USB function port allows the transmission of data to an external host, e.g. between a host PC and memory storage device.

The USB function interface is realized by the second internal host controller of the SH7724. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed-, full-speed and high-speed.

The data lines and the control line VBUS are available at the SODIMM connector. External 15-K Ω pull-down resistors are not required.

4.7 Video Out & Graphic Display

The SH7724 includes an integrated LCD controller and a video output unit (VOU).

4.7.1 Video Output

The video output unit (VOU) supports the video system NTSC with a maximum image size of 720 x 240 dots. The provided output interfaces is an 8-bit multiplexed YC interface which can be used for an external video codec.

All data and control lines are available at the SODIMM extension connector J1. Additionally the signal VOU_RST# is connected to pin 77 of the SODIMM interface and can be used as a separate reset signal for external video codecs. The signal is controlled by the SH7724 GPIO PTB1 and pulled-down by a resistor.

A 27 MHz clock for the video output unit must be supplied from the base board.

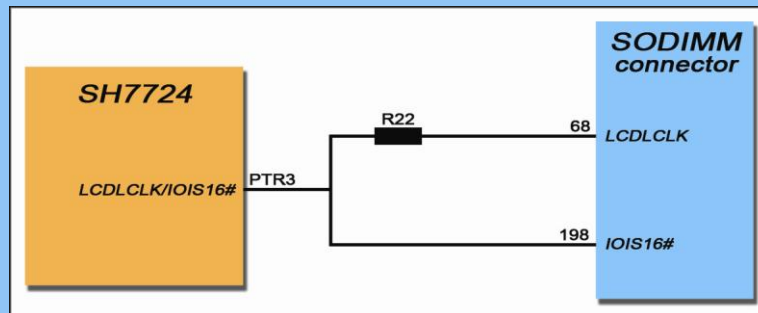
4.7.2 Graphic Display

The LCD controller of the SH7724 can drive TFT displays with resolutions up to SXGA at 24bpp. RGB- and 80-Series interfaces are supported. The pixel clock for the display data can be generated from the internal bus clock by a 64-bit pattern divider. Also an external clock can be supplied via the LCDCLK pin on the SODIMM connector. Thus all timings can individually be adapted by software to the connected display.

All data and control lines up to 18bpp color depth are available at the SODIMM connector. Please ask emtrion if 24bpp color depth is necessary.

Watch:

The LCDLCK of the SH7724 is multiplexed with the IOIS16# signal. At the SODIMM connector is one pin reserved for LCDLCLK and one pin for IOIS16#. This is why the portpin of the CPU is routed to both pins at the SODIMM connector. In addition the LCDLCLK pin on the SODIMM connector is routed via a resistor, which is soldered by default.



When the LCDLCLK input is used the IOIS16# pin on the SODIMM must be left unconnected on the base board. Please ask emtrion for DIMM-SH7724 variants without the LCDLCLK option.

4.8 Video Input

The SH7724 comes with two video input units (VIO) which can be used with different video sources, such as video codec or CMOS camera modules.

The interfaces at the DIMM-SH7724 are realised with an 8-bit data-bus and supports various input formats. The first input (VIO0) is available at the SODIMM connector; the second input (VIO1) is available at the SODIMM extension connector J1.

For applications which need more than two video inputs the signal VIO_SRC (GPIO PTA7) can be used to switch between different sources. But this must be support by the base board. Also a separate reset signal VIO_RST# (GPIO PTA6) can be used to reset video codec's at the base board. Both signals are connected to the SODIMM connector and pulled down by a resistor.

The clock for the VIO interfaces must be supplied from the base board.

4.9 Touch Interface

A 4-wire touch interface is implemented by using the AR1020 touch interface controller from Microchip [3].

The controller is connected to the I²C bus interface of the SH7724. The IRQ output of the controller is connected to IRQ2 of the SH7724. The 7-bit I²C-Address is 0x4D.

The touch interface signals are available at the SODIMM connector.

4.10 Audio Interface, SSI port

The SH7724 processor has an integrated FIFO-Buffered Serial Interface (FSI) that can be used to send and receive audio data from external audio codec's. There is also a Sound Processing Unit (SPU) with two DSPs for sound and audio processing available.

The Interface is connected to SODIMM connector, which allows the selection of an external audio codec. The input clock for the audio port must be externally supplied.

4.11 SD-Card Interface

The SH7724 includes one SD Card interfaces (SDHI) to drive memory- or I/O cards. The signals, including card detect and write protect lines, are routed with all necessary pull up resistors to the SODIMM connector.

The SDHI interface is connected to the first SD-Card interface on the SODIMM connector.

At the SODIMM connector a few pins are reserved for a second SD Card interface. These pins are connected to the MSIOF1 interface of the SH7724. With the MSIOF interface SD Cards can be used in SPI mode. The MSIOF1 interface has three slave select signals (SS#). For the second SD Card interface SS2# is used. For further information to the MSIOF interface see chapter [SPI Interface](#).

The card detect and write protect signals are handled by portpins of the SH7724:

Signal	Function	GPIO	Remarks
SDC2_CD#	Low-active card detection signal	PTA5 (input)	Pullup resisitor added
SDC2_WP#	Low-active write protection signal	PTA4 (input)	Pullup resisitor added

4.12 CAN Controller MCP2515

The DIMM-SH7724 module provides a CAN controller MCP2515 from Microchip [4] with the following key features:

- Supports CAN specification V2.0B
- 1Mb/s transfer rate
- 0-8 byte data length
- Two receive buffers with prioritization
- Three transmit buffers with prioritization
- Interrupt output

The MCP2515 is connected to the SPI interface (MISOF1) of the SH7724 and the first slave select signal SS0# is used. The maximum clock rate for the MCP2515 is limited to 10MHz.

The CAN controller is clock by a 24 MHz crystal and will be reset by the global reset. The interrupt output is connected to IRQ1 of the SH7724. The additional portpins of the MCP2515 are unused.

The transmit and receive signals are routed to the SODIMM connector. A CAN transceiver must be placed at the base board. emtrion also provides cables with integrated CAN transceivers. Please contact us for further information.

4.13 Serial Ports

The DIMM-SH7724 comes with four serial ports which are all integrated in the processor SH7724. The SCIF modules have different sized FIFOs and one of them has the option for two handshake signals.

At the SODIMM connector the interface names change to UART_A – UART_E.

An overview is shown as follows:

SH7724 interface	SODIMM name	handshake signals	FIFO size (byte)
SCIF0	UART_E	-	16
SCIF2	UART_D	-	16
SCIFA3	UART_A	RTS, CTS*	64
SCIFA4	UART_B	-	64
SCIFA5	UART_C	-	64

*Option for RTS/CTS handshake signals, please ask emtrion.

All signals are available at the SODIMM connector. UART-A has been implemented as a RS232 port. The signal lines of UART-B to UART-E have LVTTTL level and will need to be configured by external drivers. RS232 adaptors, which can be plugged to a pin header, are available from emtrion.

4.14 IrDA Interface

The SH7724 has an on-chip IrDA interface which supports baud rates up to 115200 kBaud. The receive- and transmit-pins are routed to the SODIMM connector. The IrDA-transceiver must be added externally.

4.15 RTC DS1337

Since the integrated RTC of the processor SH7724 does not have a separate power supply the RTC DS1337 from Maxim is added. It is clocked by a 32.768 KHz crystal which also serves as clock source for the processor.

The DS1337 is connected to the I²C bus interface (IIC0) of the SH7724. The 7-bit I²C-Address is 0x68. An alarm interrupt is available on IRQ5.

Via the SODIMM connector the RTC can be buffered by an external battery. For timekeeping a supply voltage between 1.3 Volt and 3.3 Volt must be supplied. The current consumption is below 0.6 µA.

4.16 I²C- Bus

The SH7724 provides two I²C bus interfaces with transmission speeds up to 400 kb/s. Both interfaces operate as master. The first interface (IIC0) is used for I²C devices located on the DIMM-SH7724 module; the second interface (IIC1) is routed to the SODIMM connector and used for external I²C- peripherals.

Two devices are connected to the first interface (IIC0):

Slave	Device	Chip Address
Real Time Clock	DS1337U+	0x68
Touch Controller	AR1020	0x4D

The SCL and SDA lines of both interfaces are pulled up with 2.2 KΩ resistors to 3.3V.

4.17 SPI Interface

The MSIOF1 module of the SH7724 is configured as SPI interface. The MSIOF1 interface has three slave select signals (SS0#, SS1# and SS2#) therefore three SPI devices can be controlled:

Slave Select	Device	Usage
SS0#	MCP2515	CAN Controller at DIMM-SH7724
SS1#	-	Routed to SODIMM connector for customer use
SS2#	SDC2 interface	Routed to second SD-Card interface at the SODIMM connector to use SD-Cards in SPI mode

The three signals SPI_SCK, SPI_MOSI and SPI_MISO are shared for all three devices. The maximum clock speed for SPI_SCK is 33 MHz (limitation by the SH7724). Connected devices can have other limitations!

4.18 General Purpose I/Os

Ten portpins of the processor, which can be used as GPIOs, are routed to the SODIMM connector.

SODIMM SIGNAL	SH7724 Port	Direction	Termination	Remarks
GPIO_0	PTA0	In/Out	not terminated*	-
GPIO_1	PTA1	In/Out	not terminated*	-
GPIO_2	PTA2	In/Out	not terminated*	-
GPIO_3	PTA3	In/Out	not terminated*	-
GPIO_4	PTB6	In/Out	not terminated*	Can also be used as TPU1
GPIO_5	PTB7	In/Out	not terminated*	Can also be used as TPU2
GPIO_6	PTR0	In/Out	not terminated*	Can also be used as TPU3
GPIO_7	PTR1	In/Out	not terminated*	Can also be used as TPU4
GPIO_8	PTX6	In/Out	internal pull-up resistor	Can also be used as IRDA_IN
GPIO_9	PTX7	In/Out	internal pull-up resistor	Can also be used as IRDA_OUT#

***Please terminate with a pull-up or pull-down on the base-board**

4.19 Timer Pulse Unit

Four of the GPIO pins can be used as PWM outputs for the Timer Pulse Unit (TPU) of the SH7724.

The following table shows which GPIOs are multiplexed with the TPU pins.

SODIMM SIGNAL	TPU Channel	SH7724 Port	Direction	Remarks
GPIO_4	TPU0	PTB6	Output	Can also be used as GPIO
GPIO_5	TPU1	PTB7	Output	Can also be used as GPIO
GPIO_6	TPU2	PTR0	Output	Can also be used as GPIO
GPIO_7	TPU3	PTR1	Output	Can also be used as GPIO

4.20 DIP Switches, Status LED

Four DIP Switches can be read via portpins of the SH7724. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0.

DIP Switch	GPIO
DIP1	PTR4
DIP2	PTR5
DIP3	PTB0
DIP4	PTE7

Watch:

The DIP-Switch can only be used with modules later than hardware revision R2A.

A bicolour LED is connected to the port pins PTJ7 and PTJ5 of the SH7724. If PTJ7 is high a green LED is lighting, if PTJ5 is high a red LED is lighting. If both ports are high both LEDs are on, which results in a yellow light.

4.21 Memory Map

The SH7724 processor provides 8 areas with 64 MByte address space whose characteristics can be individually programmed. As default address map 1 is used, then area 5 and 6 are divided into two 32 MByte blocks each. The address usage is as follows:

Area	Function	Bus Width	Area Size	Address Region
0	Up to 64 Mbyte NOR-Flash	16-bit	64 MByte	00000000 – 03FFFFFF
1	SH7724 internal I/O register	-	64 MByte	04000000 – 07FFFFFF
2	64 MByte DDR2 SDRAM	32-bit	64 MByte	08000000 – 0BFFFFFF
3	64 MByte DDR2 SDRAM	32-bit	64 MByte	0C000000 – 0FFFFFFF
4	64 MByte DDR2 SDRAM	8/16-bit	64 MByte	10000000 – 13FFFFFF
5A	32 MByte DDR2 SDRAM	16-bit	32 MByte	14000000 – 15FFFFFF
5B	32 MByte DDR2 SDRAM	16-bit	32 MByte	16000000 – 17FFFFFF
6A	SODIMM, CS6A#	8/16-bit	32 MByte	18000000 – 19FFFFFF
6B	SODIMM, CE1B#	8/16-bit	32 MByte	1A000000 – 1BFFFFFF
7	reserved	-	64 MByte	1C000000 – 1FFFFFFF

The timing characteristics of area 1 and the SDRAM areas 2, 3, 4, 5A and 5 are programmed according to the requirements of the DIMM-SH7724 processor board.

Areas 6A and 6B are reserved for external extensions and therefore configured with the slowest timing.

4.22 Interrupts

The processor SH7724 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor. Eight dedicated interrupt input pins are available for external devices.

Three interrupts lines are used for the touch controller, the CAN controller and the RTC. IRQ3 and IRQ4 are multiplexed with the SCIFA3 interface and used for the terminal interface. Therefore three interrupts lines and the NMI are available for external devices via the SODIMM connector.

The use of the interrupt inputs and the resulting interrupt code is displayed in the following table:

Name	Source	INTEVT
NMI	SODIMM	0x1C0
IRQ0	SODIMM (IRQ-A)	0x600
IRQ1	CAN (MCP2515)	0x620
IRQ2	Touch AR1020	0x640
IRQ3	not available (pin is used for SCIF3)	0x660
IRQ4	not available (pin is used for SCIF3)	0x680
IRQ5	Real Time Clock (DS1337)	0x6A0
IRQ6	SODIMM (IRQ-B)	0x6C0
IRQ7	SODIMM (pin 119)	0x6E0

4.23 DMA

The SH7724 has two integrated DMA controller with 6 channels each.

Many integrated peripherals of the processor SH7724 like the Sound Unit, SD Card Controller, USB can be operated internally with DMA transfers.

One DMA channel (DACK0/DREQ0) is available on the SODIMM connector for external devices.

4.24 Reset

There are several ways for issuing a reset signal:

- Three voltage monitors check the 3.3 Volt supply voltage of the board, the 1.3 Volt Core voltage of the processor and the 1.8 Volt DDR2 SDRAM voltage.
- Via the active low signal RESI# at the SODIMM connector
- Via the active low signal HRESI# at the Debug connector
- Via software by setting port pin PTV1 to 0
- Unstable RCLK clock (CPU main clock)

All reset sources are combined together to one reset signal RESET_CPU# which is connected to the RESETP# input of the SH7724. The minimum duration of RESET_CPU# is 1.4ms. The reset output of the SH7724 is then connected to onboard peripherals and the SODIMM connector.

4.25 Debugging interface

At the 20 pole header J3 all signals of the User Debugging Interface H-UDI and also the additional six pins for emulator connection, AUD, are available. The debugging interface can be used for example with an E10A emulator from Renesas.

Please contact emtrion for further details how to connect an emulator to J3.

4.26 Power Supply

A voltage of +3.3 volts, +/- 5%, @ typ. 0.4 A must be supplied via the SODIMM connector. Further voltages for the processor and the other parts are generated on board.

4.27 HiCO.DIMM Interface

All interface signals of the board and an SRAM like bus interface for external peripheral additions are available at the SODIMM connector which is named HiCO.DIMM interface.

The HiCO.DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2.5V keying. These sockets are available from various manufacturers.

Most of the pins are directly connected with the processor SH7724. Usage details of the connector and its electrical and mechanical characteristics can be found later in this document. For detailed electrical specification please refer to Section 44, Electrical Characteristics, in the SH7724 hardware manual [1].

Watch:

The pinout of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pinout may damage the DIMM-SH7724 and the carrier board.

5 Pin Assignments

5.1 J1, Extension Connector

Type: 30-pin connector, Hirose DF12(3.0)-30DS-0.5V (Receptacle)
Corresponding header for base boards: Hirose DF12(3.0)-30DP-0.5V

Pin	Signal	Pin	Signal
1	GND	2	+3.3 V
3	VOU_D7	4	VIO1_D7
5	VOU_D6	6	VIO1_D6
7	VOU_D5	8	VIO1_D5
9	VOU_D4	10	VIO1_D4
11	VOU_D3	10	VIO1_D3
13	VOU_D2	10	VIO1_D2
15	VOU_D1	10	VIO1_D1
17	VOU_D0	18	VIO1_D0
19	GND	20	GND
21	VOU_CLKI	22	VIO1_CLK
23	VOU_CLK	24	VIO1_FLD
25	VOU_VSYNC	26	VIO1_VD
27	VOU_HSYNC	28	VIO1_HD
29	GND	30	+3.3 V

5.2 J12, SODIMM connector

Type 200 pin SODIMM socket, 0.6 mm Pitch, 2,5V keying

Pin	Signal	Interface		Signal	Pin		
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2		
3	ETH_TDP			USBH_OC#	4		
5	ETH_TDM			USBH_DM	6		
7	GND			USBH_DP	8		
9	ETH_RDP			USB Device	USBF_VBUS	10	
11	ETH_RDM		USBF_DM		12		
13	LINK_LED#		USBF_DP		14		
15	USBH_VBUS		USB Host		Power	GND	16
17	CAN_TX		CAN		UART-A	SCIF3_TXD#	18
19	CAN_RX			SCIF3_RXD#		20	
21	SCIF0_TXD	UART-E	SCIF3_RTS#*	22			
23	SCIF0_RXD		SCIF3_CTS#*	24			
25	SCIF2_TXD	UART-D	Touch	Touch_XP		26	
27	SCIF2_RXD			Touch_XM	28		
29	SCIF5_TXD	UART-C		Touch_YP	30		
31	SCIF5_RXD			Touch_YM	32		
33	SCIF4_TXD	UART-B		A/D	n/c	34	
35	SCIF4_RXD		n/c		36		
37	n/c	A/D	n/c		38		
39	+3V3	Power		GND	40		
41	LCD_D22	LCD		LCD_D23	42		
43	LCD_D20*			LCD_D21*	44		
45	LCD_D18 *			LCD_D19*	46		
47	LCD_D16			LCD_D17	48		
49	LCD_D14			LCD_D15	50		
51	LCD_D12			LCD_D13	52		
53	LCD_D10			LCD_D11	54		
55	LCD_D8			LCD_D9	56		

57	LCD_D6		LCD_D7	58			
59	LCD_D4		LCD_D5	60			
61	LCD_D2		LCD_D3	62			
63	LCD_D0		LCD_D1	64			
65	+3V3	Power		GND	66		
67	LCDRD#	LCD		LCD_LCLK	68		
69	LCD_DISP			LCD_DCK	70		
71	LCD_HSYN			LCD_DON	72		
73	LCD_VSYN			LCD_VCPWC*	74		
75	VOU_DEST**			LCD_VEPWC*	76		
77	VOU_RST#	VIO0, VOU		VIO0_D7	78		
79	VIO0_FLD			VIO0_D6	80		
81	VIO_CKO			VIO0_D5	82		
83	VIO0_CLK			VIO0_D4	84		
85	VIO0_HD			VIO0_D3	86		
87	VIO0_VD			VIO0_D2	88		
89	VIO_SRC			VIO0_D1	90		
91	VIO_RST#			VIO0_D0	92		
93	+3V3	Power		GND	94		
95	SPI_MISO	SDC2	SDC1	SDC1_D0	96		
97	n/c			SDC1_D1	98		
99	n/c			SDC1_D2	100		
101	SPI_SS2#			SDC1_D3	102		
103	SPI_MOSI			SDC1_CMD	104		
105	SPI_SCK	SPI		SDC1_CLK	106		
107	SDC2_CD#			SDC1_CD#	108		
109	SDC2_WP#			SDC1_WP#	110		
111	SPI_SS1#			SPI_MISO	112		
113	SPI_SCK	I2C		SPI_MOSI	114		
115	SCL			Audio		AUDIO_BCK	116
117	SDA					AUDIO_LRC	118
119	IRQ7			AUDIO_DATI	120		

121	n/c		AUDIO_DATO	122
123	GND	Power	AUDIO_MCLK	124
125	IrDA_IN#	GPIO,TPU	IrDA_OUT	126
127	GPIO_G/ TPU2		GPIO_H/ TPU3	128
129	GPIO_E/ TPU0		GPIO_F/ TPU1	130
131	GPIO_C		GPIO_D	132
133	GPIO_A		GPIO_B	134
135	+3V3	Power	GND	136
137	A22	Address A[23:0]	A23	138
139	A20		A21	140
141	A18		A19	142
143	A16		A17	144
145	A14		A15	146
147	A12		A13	148
149	A10		A11	150
151	A8		A9	152
153	A6		A7	154
155	A4		A5	156
157	A2		A3	158
159	A0		A1	160
161	+3V3	Power	GND	162
163	D14	Data D[15:0]	D15	164
165	D12		D13	166
167	D10		D11	168
169	D8		D9	170
171	D6		D7	172
173	D4		D5	174
175	D2		D3	176
177	D0	D1	178	
179	CKIO	Bus Control	DREQ0	180
181	n/c		DACK0	182

183	RD#		IRQ0	184
185	RD/WR#		IRQ6	186
187	WE0#		NMI	188
189	WE1#		RESO#	190
191	ICIORD#		RESI#	192
193	ICIOWR#		CS6B#/CE1B#	194
195	WAIT#		n/c	196
197	CS6A#		IOIS16#	198
199	BAT	Power	GND	200

* These signals are not available by default. Please ask emtrion for further information.

** The signal VOUE_DEST has no function with DIMM-SH7724. It is pull-down to GND with a 10K resistor.

5.3 J3, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	AUDCK	2	TCK
3	GND	4	GND
5	AUDSYNC	6	TRST#
7	+3.3 V	8	+3.3 V
9	AUDATA3	10	TDO
11	AUDATA2	10	ASEBRK#
13	AUDATA1	10	TMS
15	AUDATA0	10	TDI
17	GND	18	MPMD
19	HRESI#	20	RESET_CPU#

6 Signal Characteristics

Abbreviations:

AI analog input
 AO analog output
 A I/O analog bidirectional
 I digital input
 O digital output
 I/O digital bidirectional

PU xK x K Ω pullup resistor
 PD xK x K Ω pulldown resistor
 SR xR x Ω series resistor
 TIU xK transistor inverter with x K Ω pullup resistor
 TID xK transistor inverter with x K Ω pulldown resistor

6.1 J1, Extension Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
VOU (Video Output Unit)					
VOU_D[7:0]	O	-	3.3	2	VOU data output
VOU_CLKI	I	-	3.3	-	VOU clock input
VOU_CLK	O	-	3.3	2	VOU clock output
VOU_VSYNC	O	-	3.3	2	VOU vsync output
VOU_HSYNC	O	-	3.3	2	VOU hsync output
VIO1 (Video Input Unit 1)					
VIO1_D[7:0]	I	-	3.3	-	VIO1 data input
VIO1_CLK	I	-	3.3	-	VIO1 clock input
VIO 1_FLD	I	-	3.3	-	Field identification signal
VIO1_VD	I	-	3.3	-	VIO1 vsync input
VIO1_HD	I	-	3.3	-	VIO1 hsync input
Miscellaneous					
+3V3	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

6.2 J2, SODIMM Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
Ethernet					
SPEED_LED#	O	-	3.3	4	100 MBit indicator
ETH_TDP	A O	-	-	-	TX diff. output pos.
ETH_TDM	A O	-	-	-	TX diff. output neg.
ETH_RDP	A I	-	-	-	RX diff. input pos.
ETH_RDN	A I	-	-	-	RX diff. input neg.
LINK_LED#	O	-	3.3	4	traffic indicator
USB Host					
USBH_PEN#	O	PU 10K	3.3	4	Power enable for switch
USBH_OC#	I	PU 10K	3.3	-	Overcurrent from switch
USBH_DP	I/O	-	3.3	-	Diff. data positive
USBH_DM	I/O	-	3.3	-	Diff. data negative
USBH_VBUS	I	-	5	-	VBUS detection
USB Device					
USBF_VBUS	I	-	5	-	VBUS detection
USBF_DP	I/O	-	3.3	-	Diff. data positive
USBF_DM	I/O	-	3.3	-	Diff. data negative
UART					
SCIF0_TXD	O	PU 10K	3.3	2	transmit data
SCIF0_RXD	I	-	3.3	-	receive data
SCIF2_TXD	O	PU 10K	3.3	2	transmit data
SCIF2_RXD	I	-	3.3	-	receive data
SCIF3_TXD#	O	-	RS232	2	RS232 transmit data
SCIF3_RXD#	I	-	RS232	-	RS232 receive data
SCIF3_RTS#	O	-	RS232	2	RS232 modem control
SCIF3_CTS#	I	-	RS232	-	RS232 modem control
SCIF4_TXD	O	PU 10K	3.3	2	transmit data
SCIF4_RXD	I	-	3.3	-	receive data
SCIF5_TXD	O	PU 10K	3.3	2	transmit data
SCIF5_RXD	I	-	3.3	-	receive data
4-Wire Resistive Touch Interface					
TOUCH_XP	A I/O	-	3.3	-	X plus terminal
TOUCH_XM	A I/O	-	3.3	-	X minus terminal
TOUCH_YP	A I/O	-	3.3	-	Y plus terminal
TOUCH_YM	A I/O	-	3.3	-	Y minus terminal
LCD Controller					
LCD_VCPWC	O	-	3.3	2	VCC power control

LCD_VEPWC	O	-	3.3	2	VEE power control
LCD_DON	O	-	3.3	2	LCD display enable signal
LCD_DISP	O	-	3.3	2	LCD display enable signal
LCD_VSYNC	O	-	3.3	2	LCD frame sync output
LCD_HSYNC	O	-	3.3	2	LCD line sync output
LCD_DCK	O	-	3.3	2	LCD pixel clock output
LCD_LCLK	I	SR 22R	3.3	-	LCD source clock (external input)
LCD_D[23:0]	O	-	3.3	2	LCD colour data
VOU (Video Output Unit)					
VOU_RST#	O	PD 10K	3.3	2	Reset signal for video device
VOU_DEST	O	PD 10K	3.3	2	No function
VIO0 (Video Input Unit)					
VIO0_D[7:0]	I	-	3.3	-	Video image input data
VIO0_CLK	I	-	3.3	-	Video clock input
VIO0_HD	I	-	3.3	-	Video hsync input
VIO0_VD	I	-	3.3	-	Video vsync input
VIO0_FLD	I	-	3.3	-	Field identification signal
VIO_CKO	O	-	3.3	2	Clock output
VIO_SRC	O	PD 10K	3.3	2	Selection of either camera or video codec input
VIO_RST#	O	PD 10K	3.3	2	Reset signal for video device
SPI					
SPI_SS1#	O	PU 10K	3.3	2	Slave select output
SPI_SCK	O	-	3.3	2	Clock output
SPI_MISO	I	-	3.3	-	Input data from slave
SPI_MOSI	O	-	3.3	2	Output data to slave
SD Card Interface 1					
SDC1_D[3:0]	I/O	PU 10K	3.3	2	SDC data
SDC1_CMD	I/O	PU 10K	3.3	2	CMD signal
SDC1_CLK	O	-	3.3	2	SDC Clock output
SDC1_CD#	I	PU 10K	3.3	-	Card detect input
SDC1_WP#	I	PU 10K	3.3	-	Write protect input
SD Card Interface 2					
SPI_SS2#	O	PU 10K	3.3	2	Slave select output
SPI_SCK	O	-	3.3	2	Clock output
SPI_MISO	I	-	3.3	-	Input data from slave
SPI_MOSI	O	-	3.3	2	Output data to slave
SDC2_CD#	I	PU 10K	3.3	-	Card detect input
SDC2_WP#	I	PU 10K	3.3	-	Write protect input
I2C					

SCL	I/O	PU 2K2	3.3	-	I ² C clock signal
SDA	I/O	PU 2K2	3.3	-	I ² C data signal
Audio					
AUDIO_MCK	I	-	3.3	-	Master clock input
AUDIO_BCK	I/O	-	3.3	2	Sound bit clock
AUDIO_LRC	I	-	3.3	-	Sound L/R signal
AUDIO_DATI	I	-	3.3	-	Sound serial input data
AUDIO_DATO	O	-	3.3	2	Sound serial output data
CAN					
CAN_TX	O	-	3.3	2	transmit data
CAN_RX	I	-	3.3	-	receive data
IrDA Interface					
IrDA_OUT	O	-	3.3	2	transmit data
IrDA_IN#	I	-	3.3	-	receive data
Timer Pulse Unit					
TPU[3:0]	O	-	3.3	2	compare output / PWM output
General Purpose I/O					
GPIO[D:A]	I/O	-	3.3	2	digital input / output
Bus Interface					
A[23:0]	O	-	3.3	2	Processor address bus
D[15:0]	I/O	SR 82R	3.3	2	Processor data bus
CKIO	O	SR47R	3.3	2	83,3 MHz bus clock
WAIT#	I	PU 1K	3.3	-	Wait Input
CS6A#	O	-	3.3	2	Chip select output
RD#	O	SR 82R	3.3	2	Read signal
WE0#	O	SR 82R	3.3	2	Write access on even address
WE1#	O	-	3.3	2	Write access on odd address
RD/WR#	O	-	3.3	2	Data direction signal
IRQ0	I	PU 10K	3.3	-	Interrupt 0 input
IRQ6	I	PU 10K	3.3	-	Interrupt 6 input
IRQ7	I	PU 10K	3.3	-	Interrupt 7 input
NMI	I	PU 10K	3.3	-	NMI interrupt
RESI#	I	PU 10K	3.3	-	Reset input from carrier board
RESO#	O	-	3.3	16	Reset output to carrier board
ICIORD#	O	-	3.3	2	PCMCIA read signal
ICIOWR#	O	-	3.3	2	PCMCIA write signal
CE1B#	O	-	3.3	2	PCMCIA chip select for even addresses
IOIS16#	I	-	3.3	-	PCMCIA 16 bit signal
DREQ0	I	PU	3.3	-	DMA transfer request

DACK0	O	PU 10K	3.3	2	DMA transfer request acknowledge
BAT	-	-	1.8 - 3.0	< 1 μ A	Battery backup input for RTC
+3.3 V	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

6.3 J3, Debugging Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
Debug Interface					
TCK	I	PU 4K7	3.3	-	JTAG clock input
TMS	I	PU 4K7	3.3	-	JTAG mode select input
TRST#	I	PD 1K	3.3	-	H-UDI reset input
TDI	I	PU 4K7	3.3	-	Data input
TDO	O	-	3.3	2	Data output
ASEBRK#	IO	PU 4K7	3.3	2	Pin for emulator
AUDSYNC, AUDCK, AUDATA[3:0]	O	-	3.3	2	Pins for emulator
MPDM	I	PU 4K7	3.3	-	ASE mode input
Miscellaneous					
RESET_CPU#	O	-	3.3	1	Reset output
HRESI#	I	PU 10K	3.3	-	Reset input
+3V3	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

7 Technical Characteristics

7.1 Electrical Specifications

Electrical Specification	
Supply Voltage	3.3 V, +/-5%
Current consumption	0.4 A typ.

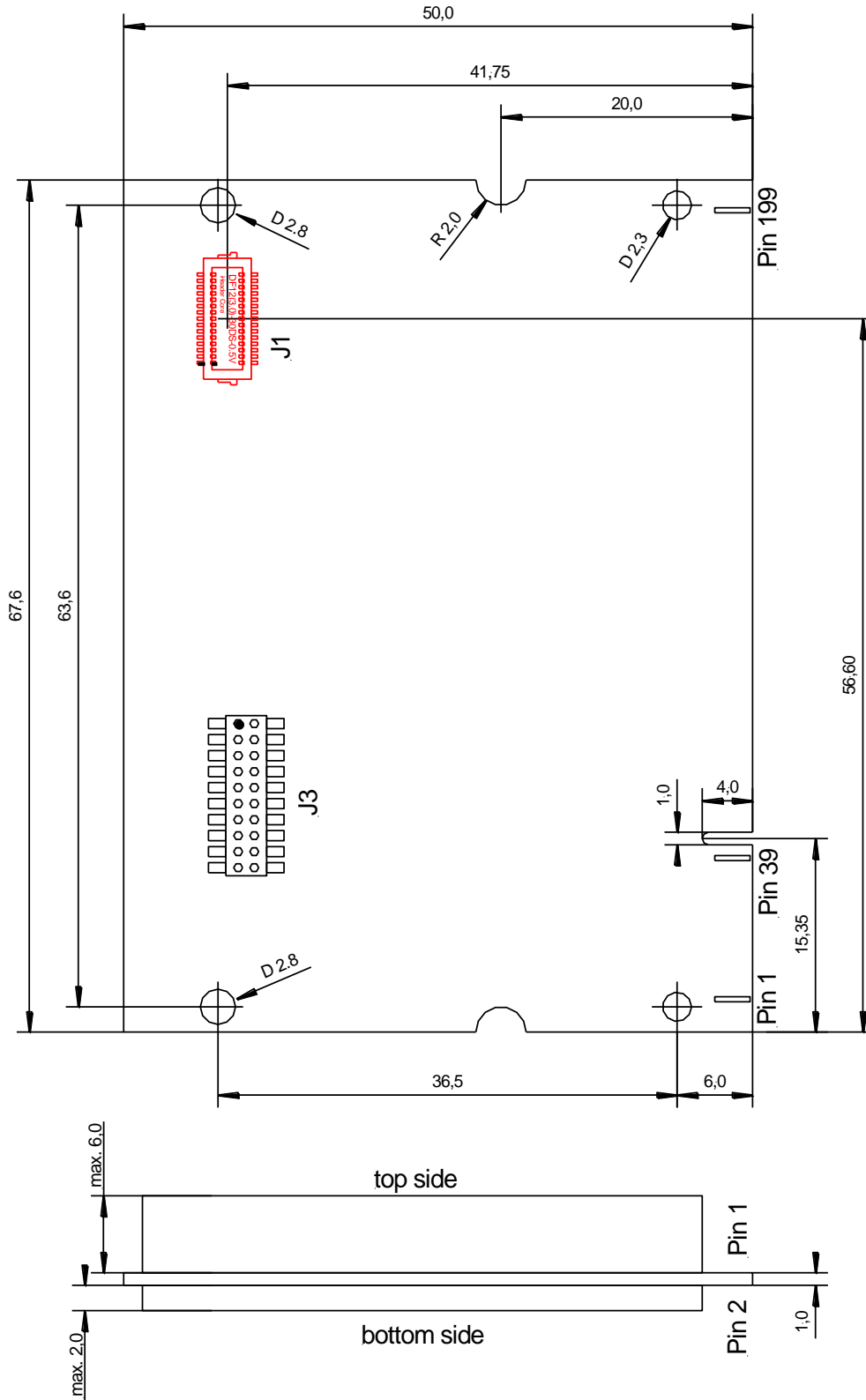
7.2 Environmental Specifications

Operating temperature	
Standard	0 ... +70°C
Extended	Please ask emtrion.
Storage temperature	
Storage temperature	-40 ... +125°C
Relative humidity	
Relative humidity	0 ... 95 %, non-condensing

7.3 Mechanical Specifications

Mechanical Specifications	
Weight	approx. 16 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 50.0 mm x 9.0 mm

7.3.1 Dimensional Drawing



Red colored parts are located on the bottom side of the CPU module.

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