

HiCO.SH3-CORE

**CPU Module with SH3DSP Processor
SH7727**

**HiCO.SH3-CORE
Manual**

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emtrion

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1 Overview

1.1 Introduction

The module HiCO.SH3-CORE is a CPU module based on the processor SH7727 (SH3DSP) from Renesas. 8/16 MByte Flash and 16/64 MByte SDRAM are available for storage.

Most of the integrated processor interfaces are directed on plug connectors to a carrier board, the so-called BASE. Besides the processor, a 10/100 Mbit Ethernet controller, two further serial interfaces, an audio interface and a freely programmable I/O block is available on the module. Their input and output signals are also directed onto the plug connectors on the carrier board.

The connectors to the base are realized according to the standard HiCO.nect from emtrion.

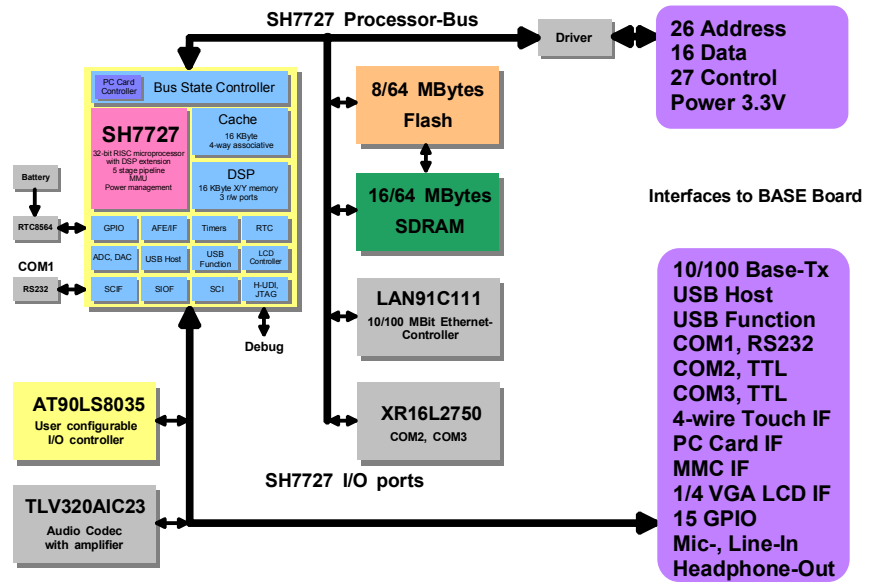
Due to the design of the module, a number of operating systems can be installed on the HiCO.SH2-CORE. Examples: Windows CE, Linux, QNX, and VxWorks.

The module is executable individually and only needs +3.4 V supply voltage for operation.

1.1 Main Characteristics of the HiCO.SH3-CORE

Characteristics	Function
Processor	SH7727-160
Flash Memory	8 / 16 MByte
Main Memory	16 / 64 MByte SDRAM
Graphics Controller	integrated in SH7727
Ethernet Controller	LAN91C111, 10/100Base-T
Interfaces	USB Host 1.1
	USB Function
	3 x COM: 1 x RS232, two of which IrDA-capable 2 x LVTTTL level
	Audio: Microphone, line in, headphone out
	PC Card Interface
	MMC Interface
	4-wire resistive touch screen
	15 x GPIO, programmable
	H-UDI, Emulator Interface
	RTC
Bus Interfaces	SH3 Processor bus
	I ² C Bus
Power Supply	0.4 A at +3.3 V
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +125°C
Dimensions	66 mm x 76 mm x 13 mm

1.2 Block Diagram



2 Module Implementation

Before you install the HiCO.SH3-CORE, please read the following important notes. These notes apply for all modules with electrostatically hazardous components. Please note the following:

- Before you touch this module you must discharge yourself. You can achieve this by touching a grounded object.
- All tools used for the installation of the module must be discharged.
- Pull the power plug of your device before installing or removing the module.
- Touch the module only at the edge of the board and do not touch any components or conductor paths.

3 Function Description

3.1 Processor

The chip SH7727-F160 is used as processor, [1], [2]. This is a 32-bit RISC processor, which is operated with an internal processor clock of 150 MHz and an external bus signal clock of 50 MHz.

The processor is operated in Little-Endian mode, to be able to support PC-compatible interfaces such as PCMCIA, and operating systems such as Windows CE.

Besides the actual CPU functions, the processor possesses a series of further functions:

- DSP function block with 16 Kbyte XY memory
- MMU with 4 GB virtual
- Clock generator with power down functions
- 16 Kbyte instruction and operand cache, 4-way set associative
- Interrupt controller with 15 levels
- Bus state controller
- Four channel DMA controller
- Three 32-bit auto-reload timer
- RTC
- USB Host Rev. 1.1
- USB Function Rev. 1.1
- LCD controller, max. 1024*1024 pixel, STN and TFT
- Analogue front-end for modem module
- Six channel 10-bit A-D converter
- Two channel 8-bit D-A converter
- Three UARTs
- PC Card Interface
- H-UDI, Debug Interface

With the HiCO.SH3, the modem interface is not used; the DMA controller is only available to the processor periphery, not to any external module.

3.2 RAM

16 Mbyte Flash and 64 Mbyte SDRAM are available for storage. The RAM is located in area 3, in the memory access space 0x0C00 0000 ... 0x0CFF FFFF for 16 MByte size, or 0x0C00 0000 ... 0x0CFF FFFF for 64 MByte size.

Both RAMS are connected in parallel for a 32 bit data bus. They are operated with 50 MHz clock and CAS latency 2.

3.3 Flash

16 Mbyte Flash are available for program storage. The Flash is located in area 0, in the memory access space 0x0C00 0000 ... 0x00FF FFFF. Strata Flash components in BGA64 package are used. With this, a maximum capacity of 64 Mbyte can be achieved.

Both flash components are connected in parallel for a 32 bit data bus.

With the signal BOOT8# on the connector to the carrier board, the area 0 can be switched to an external 8-bit memory interface. In this case, the onboard flash is turned off.

3.4 Address Map

The processor has 7 areas with 64 MB memory address space each, at a selectable data width of 8 – 32 bits. The following allocation is implemented:

Area	Function	Data capacity	Memory address space
0	Flash	32/8 Bit ***	A0000000 – A3FFFFFF
1	Internal controller	-	A4000000 – A7FFFFFF
2	Ethernet, COM2/3, Ports	16 Bit	A8000000 – ABFFFFFF
3	16 / 64 MB SDRAM	32 Bit	AC000000 – AFFFFFFF
4	External extensions	16 Bit	B0000000 – B3FFFFFF
5	External ISA bus	16 Bit	B4000000 – B7FFFFFF
6	PCMCIA	8/16 Bit	B8000000 – BBFFFFFF

*** Activating the signal BOOT8# will enable booting from the BASE from an 8-bit PROM.

3.5 Interrupts

The processor has six inputs IRQ0 ... IRQ5 for external interrupts; alternatively, four of the inputs, IRQ0 ... IRQ3, can be programmed in a way that via a 4-bit code one of the 15 interrupts is released. The code 0x1F implies no interrupt.

Except for the particular interrupt inputs, 16 port pins can be programmed as interrupt inputs PINT0 .. PINT15. The inputs PINT0 .. PINT7 and PINT8 .. PINT 15 release the same interrupt, as groups of 8 each.

For the HiCO.SH3 the four lower interrupt inputs are treated as 4-bit codes of the carrier board, to have up to 16 interrupts available for external function on the carrier

board. The Ethernet controller has its own interrupt input; the other four interrupt sources are implemented with PINT inputs.

The following allocation is implemented:

Interrupt source	Pin	Sensitivity
4-bit decoder from BASE	IRL0 .. IRL3 ..	Code
Ethernet	IRQ4	Rising edge
COM2	PINT2	High level
COM3	PINT3	High level
Touch	PINT10	Both edges
MMC	PINT11	Both edges
NMI from BASE	NMI	Rising edge

3.6 RTC

When turned off, the RTC of the processor SH7727 can not be buffered with a battery. To continue counting time and date also when the HiCO.SH3-CORE is turned off, the device RTC8564 from Epson is used.

This device has an integrated clock quartz and is buffered by a lithium battery type CR2016, which guarantees at least 10 years operation.

When turned on, the RTC8564 delivers a 32,768 KHz clock to the RTC of the SH7727. This enables synchronous operation of the internal processor clock and the external RTC.

3.7 Serial Interface COM1

Altogether, the module HiCO.SH3-CORE has three serial interfaces in various designs.

The interface COM1 is controlled by the SCIF interface of the SH7727. It has four handshake lines, with RTS, CTS, DTR, and DCD. The signals DTR and DCS are implemented with the help of the port pins PTC4 and PTC5.

The lines are directed to the BASE via a RS232 transceiver.

3.8 Audio

An audio codec TLV320AIC23 from Texas Instruments is controlled via the SIOF interface of the SH7727.

The Codec also has, besides two line inputs, a microphone input, which can be amplified internally with 20 dB, and a headphone amplifier, which can deliver 30 mW at 32 Ω.

The Codec has 10 internal registers to configure the digital and analogue interfaces, and to control the volume. The registers are controlled via the I²C bus; the I²C address is 0x1A.

All audio codec inputs and outputs are directed to the BASE.

3.9 USB Host, USB Function

The processor SH7727 has two USB function blocks. With the HiCO.SH3, one of them is operated as USB host and the other one as USB function. Both interfaces are compatible with USB 1.0.

Via the USB function, data can be transmitted to an external host. This is a full speed interface (12 Mbit) according to USB 1.0. With it, for example, active sync coupling between a PC and Windows CE can be achieved.

USB devices, e.g. keyboard and mouse, can be connected to the USB host interface. The bus power supply is fed via connector J1, pin 78 (VCC5) and limited to 0.5 A. Data transmissions are possible with low speed and with full speed. The data lines are terminated with 15 K Ω resistors against GND.

The data lines for both interfaces are directed to the BASE, together with a few control signals.

3.10 LCD Controller

The internal LCD controller of the SH7727 can control displays with up to 1024x1024 pixels with a maximum of 16-bit colour depth. It supports TFT, STN, and DSTN displays, both monochrome and colour. For displays with a maximum of 320 x 240 dots (1/4 VGA), in addition, a 90° clockwise rotation can take place per hardware.

The graphics controller does not have its own memory; the main memory is used as frame buffer. To keep the bus load as low as possible, for the HiCO.SH3 it is recommended to only connect 1/4 VGA displays with a maximum of 256 colours.

An example for such a display would be the SX09Q002-BZA by Hitachi. This is a 1/4 VGA colour STN display with a 5,7" diagonal and integrated touch screen.

To control displays larger than 1/4 VGA, an external VGA controller should be used.

As a source for the pixel clock, CKIO (50 MHz) or the quadruple USB signal pulse (48 MHz) can be used. They can be divided by 1, 2, 4, 8, or 16.

All signals to control an STN display with a maximum of eight data bits are directed to the BASE.

3.11 Touch Controller

The processor SH7727 has an integrated 10-bit A-D converter. An interface for a 4-wire touch panel is implemented by the means of the analogue inputs AN4 and AN5, and the port pins PTJ3, PTJ4, and PTJ5.

Via the port pins, the supply voltage is connected to the X and Y connectors of the touch panel, via the analogue inputs the voltage is measured in X and Y direction. The pen down recognition is implemented via the port pin PTM3, which can also cause interrupts.

The four connectors of the touch interface are directed to the BASE.

3.12 Analogue Outputs

The SH7727 has two 8 bit D-A converters, whose output voltage is 0... 3.3 V. The signals are directed to the BASE via amplifiers as analogue outputs AN0 and AN1. The maximum permissible output current is 20 mA.

The amplifiers are operated with an amplification of 1.2, through which a maximum output voltage of 3.3 V is already reached at an output value of 194. For values between 195 and 255, the output voltage will not increase and stay at 3.3 V.

3.13 PC Card Interface

The SH7727 has an integrated PCMCIA controller with one channel, over which in area 6 a PCMCIA card according to specification Rev. 2.1 can be controlled. All control signals necessary to implement an external PCMCIA or CF interface without an additional controller, are directed to the BASE board.

To get a complete PCMCIA interface, drivers for 26 address signals and 16 data signals must be added to the BASE. For a CF interface, the upper 15 addresses may be omitted.

3.14 MMC Interface

With the help of the SCI interface of the SH7727, an interface for Multi Media Cards (MMC) is realized. With it, MMCs can be controlled in the SPI mode.

Via the port pin PTF3 (PINT11), a card detect signal is additionally realized; the port pin PTJ1 is used as chip select output.

Due to space limitations, no MMC socket exists on the HiCO.SH3-CORE. All signals are directed to the BASE.

3.15 I2C Bus

An Inter-IC-Bus (I^2C bus) is controlled by the data bits 0 and 1 at the address 0xA8000040. The bus exists of a bi-directional data line SDA and a bi-directional clock line SCK, to which all participants are connected in parallel. For each data transmission, one participant is the master, and a second participant is the according slave. This allocation is always only valid for the duration of a telegram. There is no fixed master; theoretically each participant can start a data transmission as master. The slave is selected by the master by sending an address byte; this is the reason why each slave address may only exist once at the bus. On the HiCO.SH3-CORE, the addresses 0x51 and 0x1A are reserved; these addresses may not be used externally any more.

For the HiCO.SH3-CORE the Bit 0 is SCL and bit 1 is SDA. When writing a 0, the line is driven; when writing a 1, the line stays in high impedance and is pulled to high level by a pull-up resistor. The frequency of the clock line is determined by the software and is typically 150 KHz.

The bus is directed to the BASE via 5V-tolerant bi-directional drivers. There, the bus can be used to control 5V or 3.3V components through suitable pull-up resistors.

3.16 Serial Interface COM1

With a device XR16L2750, two more serial interfaces are implemented on the HiCO.SH3-CORE. The interfaces are basically compatible to 16550, but have 64-byte deep FIFOs. In addition, both interfaces can directly control external IrDA transceivers. For this, the IrDA mode of the interface must be activated through software.

The lines TxD, RxD, RTS, and CTS are directed to the BASE as LVTTTL signals.

In addition, COM3 is used as internal connection to a second AVR microcontroller. For this, with the output signal DTR from COM3, the receiving line can be switched between receiving from the BASE and receiving from the AVR. Sending always takes place to both participants.

For receiving, the following applies:

DTR, COM3	Interface
0	AVR
1	BASE

The DUART is supplied with a 3.684 MHz clock, from which the baud rates are derived. Compared with a standard PC, the baud rate is higher by the factor 2.

COM2 has the basic address 0xA8000080 and goes to interrupt PINT2; COM3 has the basic address 0xA80000C0 and goes to PINT3. The registers are addressed 8-bit wide at all even addresses.

3.17 Binary Inputs and Outputs

The hardware version of the HiCO.SH3-CORE module is read via the three port pins PTM0, PTM1, and PTM2 of the SH7727.

The position of the jumper W1 can be read via the port pin PTG4. This pin can be pulled to 0. The position of the jumper determines the start behaviour of the Bootloader of the HiCO.SH3.

A green and a yellow LED are controlled via the port pins PTJ6 (yellow) and PTJ7 (green). If the output is 0, the LEDs light up.

3.18 AVR Microcontroller

A second microcontroller ATMEGA8535L-8Ai (AVR) from Atmel is available for additional inputs and outputs. The 15 port pins PA7..PA0, BP0, PB1, PD7..PD4, and PD2 of this microcontroller are directed to the BASE for customer use.

In addition, the four port pins PC3..PC0 are directed to the BASE. They are used to code a BASE hardware version, but they can also be used otherwise.

All port pins can be programmed as digital input or digital output. Alternatively, the pins of Port A can be operated as analogue inputs with 10-bit resolution and a voltage range of 0 .. 2.5 V. Alternatively, the pins of Port D can be operated as PWM output, as interrupt input or as timer output. The pins PB0 and PB1 can be configured as counter inputs.

Further information regarding the characteristics and the programming of the port pins can be found in the device manual [4].

A communication between the AVR and the SH7727 is realised on-board via the serial interface COM3. The AVR is clocked with 3.684 MHz. To be able to receive data from the AVR, the line DTR of the COM3 must be set to one; the according UART bit must be programmed with 0.

The programming of the internal flash of the AVR can take place from the outside via the programming connector J4, or from the SH7727 via a local SPI interface. With this, a firmware download can be implemented via the Bootloader of the HiCO.SH3.

The SPI interface is implemented via a port at the address 0xa8000000. The data bits have the following meanings:

Bit	Meaning for Read	Meaning for Write
0	MISO	If SPI enabled: SCK
1	Always 1	If SPI enabled: RESET#
2	Always 1	If SPI enabled: MOSI
3	Always 1	0 = SPI disabled 1 = SPI enabled
4..15	Always 1	-

When SPI is enabled, the AVR can be set to reset by RESET# = 0 also without further employment of the SPI interface.

The advantage of this solution is the high flexibility. Via the second microcontroller, besides simple analogue and digital I/Os also complex functions such as a keyboard matrix decoder or a PS/2 interface can be easily implemented.

3.19 Ethernet Controller

The Ethernet controller is realised with the SMSC device LAN91C111. The chip contains the media access controller (MAC) as well as the physical layer interface (PHY) in one single chip and has an integrated SRAM with 8 Kbyte for the buffering of sender and receiver telegrams. The controller can set itself automatically to the operating states 100 BASE-TX or 10BASE-T, each half or full duplex.

The Ethernet controller is connected with a 16-bit data bus in area 2. The basic address is fixed on 0x300 in this area. There it reserves 16 consecutive addresses.

The configuration data and the MAC address must be re-programmed after each reset of the HiCO.SH3-CORE. No EEPROM is available for permanent storing of data.

Besides the four transmission lines, the status signals Link and 10/100 Mbit to control LEDs are also directed to the BASE. A suitable transformer is necessary for the connection to a RJ45 jack.

3.20 Bus Interface, Plug Connector to BASE

To extend the HiCO.SH3-CORE, addresses, data and control signals of the processor are directed to the BASE via type 74ALVT162245 drivers. All signals are located on an 80-pin plug.

On the base, the chip selects for area 0, area 2 and area 4 are made available for components. The data bus is limited to 16 bit; the memory address space is limited to 26 bit per area.

The chip select for area 0 is, together with the control signal BOOT8# used to control an external boot prom with an 8-bit data bus. This can, for example, include a

monitor for implementation or diagnostic functions, and is addressed instead of the on-board flash.

Besides the bus plug, two additional 50-pin plugs are used to direct the signals of all interfaces to the BASE.

More information regarding plugs and signals can be found in the manual HiCO.nect.

3.21 Debug Interface

The signals of the H-UDI interfaces of the processor SH7727 are directed to the connector J4. An emulator can be connected there with a suitable cable. Details for the connection of an emulator can be found in the according manual.

3.22 Power Supply, Reset

The module HiCO.SH3-CORE needs +3.3 V for the supply at a maximum power supply current of 0,4 A. The supply voltage is fed via the BASE connectors. An additional supply voltage of +1.8 V for the processor is created internally via a DC/DC converter.

To control the supply of the USB host interfaces, +5 V must be fed on connector J1, pin 78 (VCC5). It is directed to the interface via a voltage switch with overload limitation. If this is not used, the +5 V need not be fed.

A voltage monitor checks if the voltages 3.3 V and 1.8 V lie within the permissible tolerance of +/-10%. If one of the voltages exceeds the range, the processor receives a reset signal. The reset stays active for additional 200 ms after all voltages have reached the permissible range.

Besides the voltage monitor, there are three further sources for a hardware reset:

- Reset signal from the BASE module
- Reset by the port pin PTM3 of the processor
- Reset signal from the emulator connection

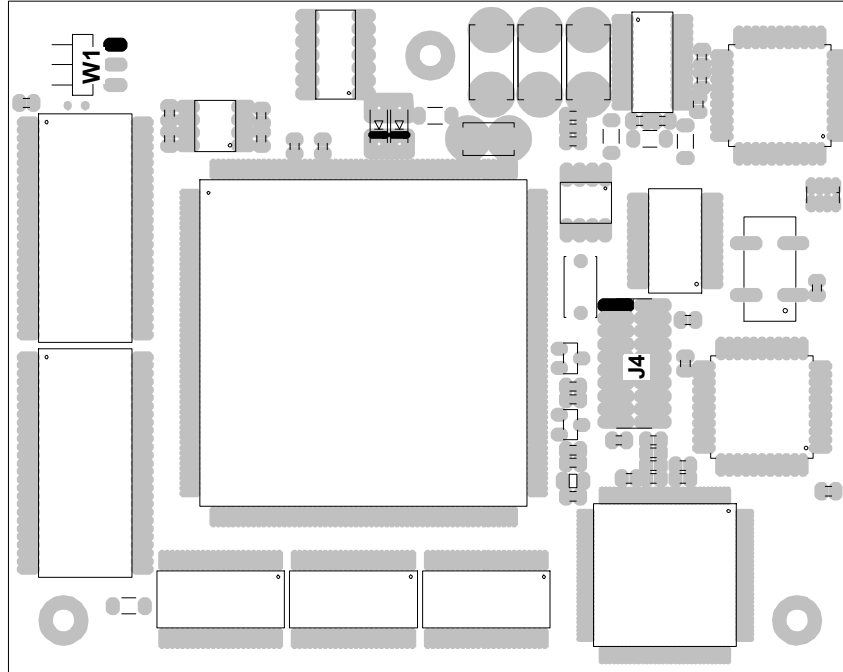
Reset can also be triggered through external connections via a pin from the BASE. The reset input RESI# is terminated with a 10 K Ω against +3.3 V and can be controlled with an open collector output.

The reset by the port pin PTM3 takes place in a way that both the bits in the port M control register are programmed to "Other function". This immediately triggers a reset. After the reset, the pin is again an input with pull-up.

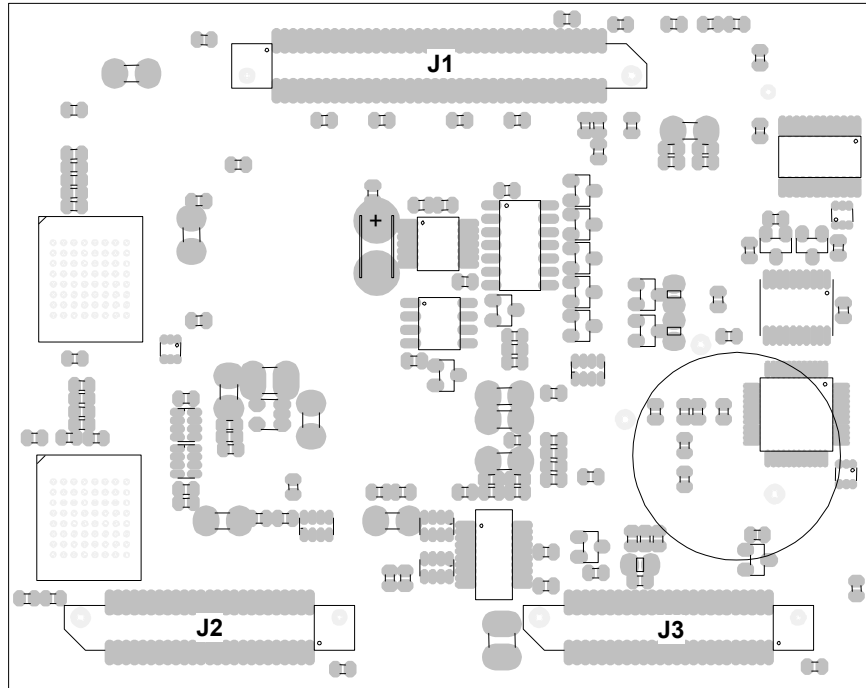
The reset input from the emulator is connected on J4 together with the H-UDI signals.

4 Location of Connectors

4.1 BS



4.2 LS



5 Connector Assignment

5.1 J1, Connection to the Base Board

Type Hirose Fx6-80P, 80-pin

Pin	Signal	Pin	Signal
1	GND	2	VCC3
3	ID0	4	ID1
5	ID2	6	ID3
7	A0	8	A1
9	A2	10	A3
11	A4	12	A5
13	A6	14	A7
15	A8	16	A9
17	A10	18	A11
19	A12	20	A13
21	A14	22	A15
23	A16	24	A17
25	A18	26	A19
27	A20	28	A21
29	A22	30	A23
31	A24	32	A25
33	GND	34	VCC3
35	D0	36	D1
37	D2	38	D3
39	D4	40	D5

Pin	Signal	Pin	Signal
41	D6	42	D7
43	D8	44	D9
45	D10	46	D11
47	D12	48	D13
49	D14	50	D15
51	GND	52	VCC3
53	DRQ	54	CLK
55	DACK#	56	BS#
57	IRQ0	58	RD#
59	IRQ1	60	WR#
61	IRQ2	62	WE0#
63	IRQ3	64	WE1#
65	NMI	66	WAIT#
67	RESO#	68	CS2#
69	RESI#	70	CS1#
71	CS0#	72	GND
73	BOOT8#	74	SDA5
75	MD4	76	SCL5
77	BAT	78	VCC5
79	GND	80	VCC3

5.2 J2, Connection to the Base Board

Type Hirose Fx6-80P, 50-pin

Pin	Signal	Pin	Signal
1	ENAVEE	2	GND
3	ENAVDD	4	REG#
5	DOFF#	6	VS1#
7	M	8	VS2#
9	FLM	10	RDY/BSY#
11	CL1	12	CE1#
13	CL2	14	CE2#
15	LCD0	16	RESET
17	LCD1	18	PDRV#
19	LCD2	20	BVD1
21	LCD3	22	BVD2
23	LCD4	24	CD1#
25	LCD5	26	CD2#
27	LCD6	28	WAIT#
29	LCD7	30	GND
31	GND	32	I_CE1#
33	ANA0	34	I_CE2#
35	ANA1	36	IOIS16#
37	GND	38	IORD#
39	MMC_IRQ	40	IOWR#
41	VCC3	42	GND
43	MMC_CS#	44	TOUCH_X1
45	MMC_SCLK	46	TOUCH_X2
47	MMC_DI	48	TOUCH_Y1
49	MMC_DO	50	TOUCH_Y2

5.3 J3, Connection to the Base Board

Type Hirose Fx6-80P, 50-pin

Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO8
3	GPIO1	4	GPIO9
5	GPIO2	6	GPIO10
7	GPIO3	8	GPIO11
9	GPIO4	10	GPIO12
11	GPIO5	12	GPIO13
13	GPIO6	14	GPIO14
15	GPIO7	16	TXD2
17	GND	18	RXD2
19	TXD1#	20	RTS2
21	RXD1#	22	CTS2
23	RTS1#	24	TXD3
25	CTS1#	26	RXD3
27	DTR1#	28	RTS3
29	DCD1#	30	CTS3
31	ETH_LED0#	32	AGND
33	ETH_TDP	34	MIC
35	ETH_TDM	36	LINE_L
37	GND	38	LINE_R
39	ETH_RDP	40	HEAD_L
41	ETH_RDM	42	HEAD_R
43	ETH_LED1#	44	USBF_PU
45	USBH_5V	46	USBF_5V
47	USBH_DM	48	USBF_DM
49	USBH_DP	50	USBF_DP

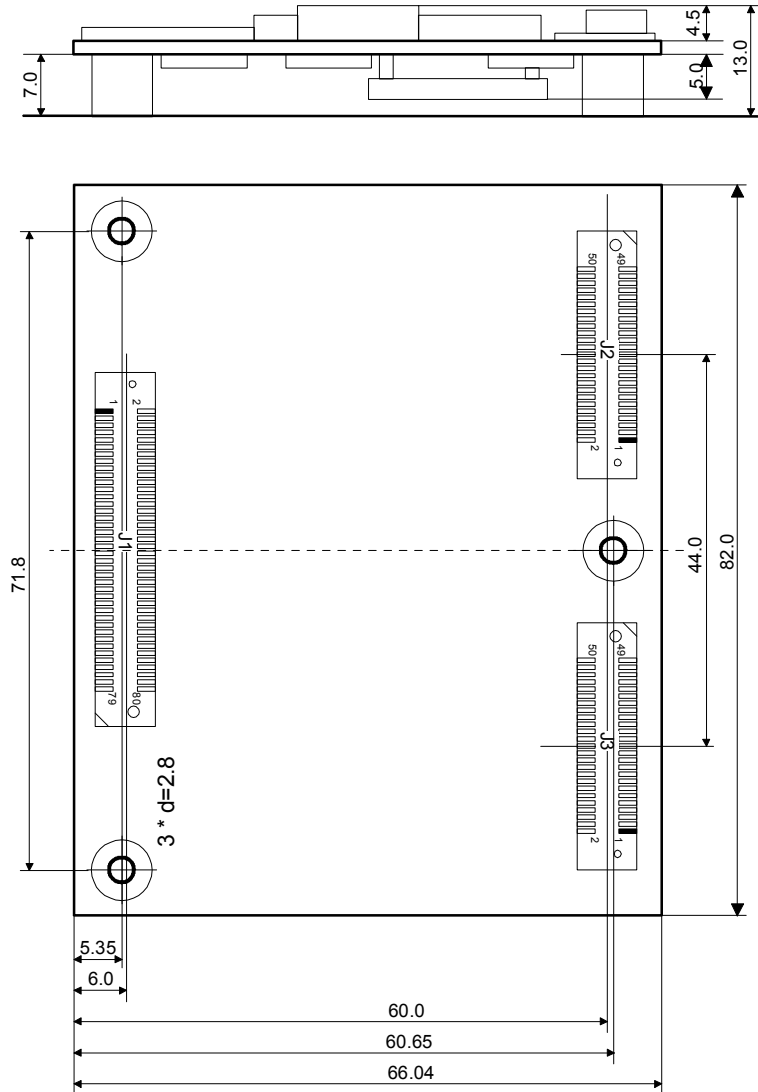
5.4 J4, Debug Connection

Type 20-pin header, 1,27mm * 1,27 mm pitch

Pin	Signal	Pin	Signal
1	+3,3 V	2	+3,3 V
3	TCK	4	GND
5	TRST#	6	ASEMOD#
7	TDI	8	TDO
9	ASEBRKAK#	10	RESET#
11	TMS	12	HRESI#
13	ATDI	14	ATDO
15	ATCK	16	GND
17	MISO	18	MOSI
19	SCK	20	RES#

6 Dimensional Drawing

Side view and view from BS through the circuit board



7 Technical Data

7.1 Mechanical Data

Weight:	36,5 g
Circuit Board:	Glass epoxy FR-4, UL listed, 6 layers
Dimensions:	66 mm x 76 mm x 11 mm

7.2 Electrical Data

Supply Voltage:	3.3 V, +/- 5%
Power Supply Current:	0.4 A max

7.3 Environmental Conditions

Temperature	Operation: 0 ... +70 °C. Storage: -40 to +125 °C
Rel. Humidity	0 ... 95 %, non- condensing

8 Additional Information

- [1] Hitachi SuperH™ RISC engine
SH7727
Hardware Manual
Revision 4.0, January 2003
Renesas
- [2] Hitachi SuperH™ RISC engine
SH3/SH3-E/SH3-DSP
Programming Manual
Revision 3.0, September 2000
Hitachi Ltd.
- [3] HiCO.nect.DOC
Design guidelines connection CORE with BASE boards
Revision 3, July 2003
emtrion
- [4] ATmega 8535, ATmega8535L
Advance Information
Rev. 2502B-AVR, September 2002
Atmel