

HiCO.SH3

CPU Module with SH3-DSP Processor

**HiCO.SH3-DOC
User Manual**

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emtrion

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emtrion GmbH

Greschbachstr. 12

D-76229 Karlsruhe

<http://www.emtrion.com>

mailto: mail@emtrion.de

Tel: +49 (0)721 62725-20

Fax: +49 (0)721 62725-19

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1. Mechanical Design

To connect the circuit boards, an 80-pin connector with the signals of the processor bus, and two 50-pin connectors with I/O signals are used.

The new connector assignment has been designed in a way that in the future other CORE modules can be implemented with the same connector assignment. To accomplish this, the 80-pin connectors are fully defined; for the I/O connectors, pins are declared as reserved, which can vary for different boards.

The distance between the HICO.SH3-CORE and the HICO.SH3-BASE is 7mm. The upper side of the HICO.SH3-CORE may only be equipped with modules equal or less than 3 mm of height. This results in other PC/104 modules easily being able to be plugged on top, without any extra measurements. High modules, like a battery or the coil of the DC/DC converter will be plugged onto the bottom.

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2. HiCO.SH3-CORE Module

2.1. HD6417727F160 Processor

2.1.1. General

The HD6417727F160 is used as a processor. This is a SH7727 with a 160 MHz processor clock in a 240-pin QFP enclosure.

2.1.2. Supply Voltage

The processor needs the supply voltages 3.3 V at typ. 20 mA and 1.8 V at typ. 330 mA and max. 650 mA. The 3.3 V supply is fed into the HiCO.SH3-CORE module from the outside; the 1.8 V are created by a DC/DC converter.

2.1.3. Clocks

The clock for the Audio Codec (49.152 MHz), the USB controller (48 MHz), the Fast Ethernet (25 MHz), and the processor are derived from a 25 MHz crystal. As the input clock is 25 MHz, a stable output clock for the Ethernet controller is available.

Due to the possible PLL settings of the processor and the external PLL, the following reasonable frequency combinations are possible:

Clock	66.66 MHz	50 MHz	40 MHz	12 MHz
PLLs	2:1:½	3:1:½	4:1:1	12:4:2
Processor	133.3 MHz	150 MHz	160 MHz	144 MHz
Bus, CKIO	66 MHz	50 MHz	40 MHz	48 MHz
Int. peripherals	33 MHz	25 MHz	40 MHz	24 MHz

The board is realised with a 50MHz input clock, because here the memory clock is 20 % higher than for the variant with a 40 MHz input clock, with the processor clock being only 6 % lower.

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The PLLS are operated in mode 9; CKIO2 is used as a clock for the SDRAMs. After being reset, the processor starts with PLL factors 1:1:¼ and must be reprogrammed to the correct frequencies.

2.1.4. Interrupts

The processor has six inputs IRQ0 .. IRQ5 for external interrupts; alternatively, four of the inputs, IRQ0 .. IRQ3, can be programmed in a way that via a 4-bit code one of 15 interrupts is released. The code 0x1F implies no interrupt.

Caution:

The input IRQ5 cannot be used with the HiCO.SH3, because the pin is used as CTS signal for COM1.

Except for the particular interrupt inputs, 16 port pins can be programmed as interrupt inputs PINT0 .. PINT15. The inputs PINT0 .. PINT7 and PINT8 .. PINT15 activate, as groups of eight each, the same interrupt.

For the HiCO.SH3 the four lower interrupt inputs are treated as 4-bit code, to have up to 16 interrupts for the HICO.SH3 BASE available. The Ethernet controller has its own interrupt input; the other four interrupt sources are implemented with PINT inputs. They are assigned as follows:

Interrupt source	Pin	Sensitivity
4-bit interrupt decoder on HICO.SH3 BASE	IRL0 .. IRL3	Code
Ethernet	IRQ4	Rising edge
COM2	PINT2	High level
COM3	PINT3	High level
Touch	PINT10	Both edges
MMC	PINT11	Both edges
NMI of the HICO.SH3 BASE, IOCHCK# on PC/104	NMI	Rising edge

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Caution:

The interrupts PINT2/PINT3 and PINT10/PINT11 activate a common interrupt each. The interrupt handler must determine the cause by means of the port signals; simultaneous interrupts must be recognized as well. The interrupts are level sensitive; the level can be programmed.

Finally, there is also the NMI input, which works independently from the other interrupts. The NMI is directed to the HiCO.SH3 BASE and is available there. In idle condition, the NMI line is on low level.

2.1.5. Address Allocation

The processor has 7 areas with 64 MB memory address space each, at a data capacity of 8 – 32 bits. Area 0 is always the boot prom. Area 1 is reserved for the internal periphery of the processor and not available externally. Only the areas 2 and 3 can drive SDRAM, and only the areas 5 and 6 can form a PCMCIA interface.

The following allocation is implemented:

Area	Function	Bus capacity	Wait states	Address range
0	Flash	32/8 Bit ***	6/2 ****	A0000000 – A3FFFFFF
1	Internal controller	8/16/32 Bit	-	A4000000 – A7FFFFFF
2	Ethernet, COM2/3, ports	16 Bit	3	A8000000 – ABFFFFFF
3	16 / 64 MB SDRAM	32 Bit	CAS 2	AC000000 – AFFFFFFF
4	Extensions on HiCO.SH3 BASE	16 Bit	3, (10 for SH4DBG)	B0000000 – B3FFFFFF
5	ISA bus	16 Bit	8 *****	B4000000 – B7FFFFFF
6	PCMCIA	8 / 16 Bit	10	B8000000 – BBFFFFFF

*** From the HiCO.SH3 BASE, an 8-bit PROM can be booted via the activation of the BOOT8# signal.

**** Burst access, primary access with 8 wait states, and then 2 wait states.

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**** The actual wait states are determined by the ISA bus controller, depending on the access. Eight wait states will be programmed.

2.1.6. Bus Interface Unit

The bus interface unit is difficult to use at a 50 MHz bus clock because of the large timing tolerances. The Read and Write timings of most of the modules are therefore created via a PLD. A clock-synchronous READ and WRITE start is only possible with the start of TW2, as for the start of TW1 the signals cannot be valid yet ($t_{RSD} < 10$, $t_{WED} = 1..10$). With the synchronous output of READ and WRITE starting at TW2, a set-up time for chip select and addresses > 27 ns ($2 * \text{clk}$ (40 ns) – t_{AD} (1,5 .. 13 ns) + PLD time (min 0)) is offered. For the DUART XR16L2750 and for the Ethernet controllers LAN91C111 10 ns each are required.

The data-hold time after the end of write is too short with the SH7727. There are several requirements; one of them is $t_{WDH3} > 2$ ns, data hold after write inactive. The Ethernet controller LAN91C111 requires $t_{5A} > 5$ ns, the DUART XR16L2750 also requires $t_{DH} > 5$ ns. For this, WRITE pulse for the periphery is ended one clock earlier.

The flash devices 28F640J3A require a minimum write high time of $t_{WPH} > 30$ ns. This is guaranteed by stopping WRITE after 4 wait states, as area 0 is programmed for read access with 6 wait states.

The DUART XR16L2750 requires an address-hold time t_{AH} of > 10 ns, also for read. The SH7727 only guarantees a hold time t_{AH} of > 7 ns. READ for the DUART must therefore be stopped one clock earlier; the data is stored temporarily in a bidirectional transceiver with a latch of type 74LVT543.

The data-hold time of the DUART $t_{DD} > 35$ ns and the interval time between two commands $t_{DY} > 40$ ns are achieved by modified timing of the signals RD# and WR#, and via a programmed idle state for area 2.

2.1.7. DMA

The DMA cannot be used for external modules, as the according pins are reserved for PCMCIA functions. The usage of DMA for the internal periphery is determined by the software.

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2.1.8. Timer

The processor has three 32-bit timers with a maximum 2 MHz input clock. The input clock is derived from a prescaler of the periphery clock. The software determines the usage of the timers.

2.1.9. Real Time Clock (RTC)

The internal real time clock of the processor is only used for the runtime, because it cannot easily be buffered by a lithium battery. The supply voltage must be 1.8 V; the power consumption is not exactly determined, but is assumed at a minimum of 50 μ A.

The real time clock is therefore implemented by the means of the Epson chip RTC8564. The module is buffered by a 3V lithium battery and has an input of 0,5 μ A. The output clock of the external run time clock is fed into the real time clock of the processor, to ensure synchronous running of both clocks.

The real time clock is addressed via an I²C bus (see section 3.7).

2.1.10. SCI

The SCI interface can be used as synchronous or asynchronous interface, without handshake signals.

Hitachi offers a solution for MMC interfaces via the SCI of the processors. This solution was incorporated for the HiCO.SH3 and is described in section 3.5.

2.1.11. SCIF

The SCIF is implemented as standard RS232 interface with RTS, CTS, DTR, and DCD. Furthermore, the signals DTR and DCD are implemented by the means of the port pins PTC4 and PTC5.

The signals are driven via a RS232 transceiver SP3243E and directed to the HiCO.SH3 BASE via the COM1 interface. The transceiver is operated in auto shutdown mode. It shuts off autonomously, when no receiving station is connected; shutting the transceiver down via software is not necessary.

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2.1.12. SIOF, Audio

An Audio Codec TLV320AIC23 by Texas Instruments is controlled via the SIOF interface of the SH7727.

The Codec also has, besides two line inputs, a microphone input, which can be amplified internally with 20 dB, and a headset amplifier, which can deliver 30 mW at 32 Ω. The Codec has 10 internal registers to configure the digital and analogue interfaces, and to control the volume. The registers are controlled by the I2C bus; the I²C address is 0x1A.

The SH7727 is operated as master; the TLV320AIC23 is operated as slave.

From the view of the SH7727, the transmission takes place in master mode 2, MSB first, with 16 bit stereo data and 32-bit frame length. The mode register SIMDR is initialised with 0xDC00.

The Audio Codec registers are, as an example, initialised with the following values:

Register	Name	Value	Meaning
6	Power Down Control	0x00	All on
4	Analogue Audio Path Control	0x15	Output only from DAC, Input from microphone, 20 dB boost on
5	Digital Audio Path Control	0x07	48 kHz de-emphasis, ADC high pass filter
7	Digital Audio Interface Format	0x11	Slave, no LR-swap, right channel on LRCIN low, 16 Bit Data, MSB first, left aligned
8	Sample Rate Control	0x00	ADC and DAC sample rate = 48 kHz
9	Digital Interface Activation	0x01	Active
0	Left Line Input Volume Control	0x117	Left/right volume simultaneous, 0 dB
1	Right Line Input Volume Control	0x117	Left/right volume simultaneous, 0 dB
2	Left Headset Volume Control	0x1E8	Left/right volume simultaneous, -17 dB

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3	Right Headset Volume Control	0x1E8	Left/right volume simultaneous, -17 dB
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The listed sequence should be observed when initialising. This applies especially to the digital interfaces.

The line inputs, the microphone input, and the amplifier outputs are directed to the HiCO.SH3 BASE.

2.1.13. AFEIF

The AFEIF is a modem interface especially for the STMicroelectronics module STLC7550. The implementation of such a modem is not planned; the pins are not connected.

2.1.14. USB Host, USB Function

The processor has three USB interfaces, which are directed outwards by two transceivers. The transceiver 2 is adherent to the USB host 2. The transceiver 1 is connected via a multiplexer either with the USB host 1 or with the USB function interface. Switching of the multiplexer during operation is not possible; it must therefore be defined, if two USB hosts or one USB host and one USB function will be used.

The second variant is used. This results in the possibility of, on the one hand, connecting the module to a host using the USB function interface, e.g. for Windows CE via Active Sync with a PC. On the other hand, USB devices can be connected to the host interface, such as a keyboard or a mouse.

For the USB function, the integrated transceiver is used. This is a full speed interface (12 Mbit) according to USB 1.0. The selectable pull-up resistance at D+ and the recognition of the connected host is implemented according to the Hitachi circuit design proposition 3.

The control of the 5 V supply of the USB host interface is implemented via an external module LM3525M-L according to the Hitachi circuit design proposition 1.

For the USB interface, an input clock of 48 MHz is fed.

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2.1.15. LCD Controller

The internal LCD controller can control displays with up to 1024x1024 pixels with a maximum of 16-bit colour depth. It supports TFT, STN, and DSTN displays, both monochrome and colour. For displays with 320x240 pixels, a 90 ° clockwise rotation is possible via the LCD controller.

The main memory of the processor is used as a frame buffer. Each time the LCD controller accesses the memory the processor is stopped. This results in a noticeable performance loss of the processor. According to Hitachi, at 66 MHz with 16 bpp, VGA resolution and 70 Hz screen refresh, the LCD controller reduces the processor performance by 45 %. At 8bpp the loss is still at 22 %.

Accordingly, a ¼ VGA display reduces the loss to ¼ of the specified values, so that such a display is barely noticed as burden. A possible display would be the DGA-32240-17-WFBLW-H. This is a ¼ VGA monochrome STN display with an extended temperature range of -20 ° - +75 °. Another display would be the SX14Q001-ZZA by Hitachi, which is a ¼ VGA colour display with a 5.7" diagonal, however, with three cables.

For displays larger than ¼ VGA, an external VGA controller is recommended.

As a source for the pixel clock, CKIO or the USB clock can be used. This makes 50 MHz and 48 MHz available, which can be divided by 1, 2, 4, 8, or 16.

2.1.16. A-D Converter

The processor has a 10-bit A-D converter with a multiplexer for six inputs. The inputs AN6 and AN7 occupy the same pins as both the analogue outputs DA0 and DA1, which results in only four analogue inputs being utilizable.

The conversion time of the converter depends on the periphery clock and is approximately 8 µs at 33 MHz. The input voltage range is 0 .. 3.3 V.

The analogue inputs AN4 and AN5 are, together with three digital outputs, used for a touch interface. This solution has already been offered by Hitachi for the R2 design and on an Epson baseboard for the SH card. The touch interface is described in section 3.9.

The analogue inputs AN2 and AN3 are not used.

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2.1.17. D-A Converter

The processor has two 8-bit D-A converters with an output voltage of 0 .. 3.3 V. The signals are directed to the HiCO.SH3 BASE via OPAMPs of LMV358 as ANA0 and ANA1. The admissible output current of the OPAMPs is 20mA.

As the OPAMPs allow a maximum input voltage of 2.5 V at 3.3 V supply voltage, they are connected with 1.2 amplification. The maximum output value for the D-A converters is therefore 194.

2.1.18. PC Card Controller

The processor has an integrated PCMCIA controller with one channel. With it, via area 6 a PCMCIA card can be controlled. This is used for an external PCMCIA or CF interface. For this, besides data and address signals, 17 control signals are directed to the HiCO.SH3 BASE board.

To receive a complete PCMCIA interface, drivers for 26 address signals, 16 data signals and 15 control signals must be placed on the HiCO.SH3 BASE. For a CF interface, the upper 15 addresses can be omitted.

Caution:

Because of duplicate allocation of the pins CD1#, CD2#, BVD1#, BVD2#, RDY, and WAIT# on the PCMCIA interface with pins of the AUD interface, no emulator with an AUD interface can be connected. There are no restrictions for emulators with H-UDI interfaces.

2.2. Memory

For the RAM, 16/64 MB SDRAM are implemented. The configuration of 16 MB or 64 MB takes place via four resistors. The RAMs are operated at a 32-bit data bus with 50 MHz at CAS latency 2.

For the flash, Intel Strata Flash or Sync Strata Flash modules in BGA64 design are used. With this, currently a capacity of 64 Mbyte can be achieved with two chips. The two flash modules are connected parallel as 32-bit data bus.

To increase the performance, the read access should take place as burst access. For this, after a reset, the page mode must be enabled in the flash with RCR.16, and the bus interface of the SH7727 for area 0 is switched to burst mode. For the

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first access, 8 wait states are necessary; the burst accesses take place with 2 wait states. Writing always takes place with 8 wait states.

To achieve a write-low time of 70 ns minimum and a write-high time of 30 ns minimum, the timing of the write signal is created by a PLD. For this, area 0 must be programmed with 5 wait states.

There is no hardware write protection for the flash modules!

2.3. PCMCIA, MMC

The SH3-DSP has an internal PCMCIA controller with one channel to realize one PCMCIA interface. The 14 control signals of the PCMCIA controller are directed to the HICO.SH3 BASE. Data and address lines on the HICO.SH3 BASE must be driven with type 74LVT245 drivers. A supply voltage switch can be implemented by the means of one or more port pins on the HICO.SH3 BASE, if necessary.

Hitachi offers the complete implementation of an MMC interface based on the SCI processor interface; this connection is incorporated for the HiCO.SH3. The MMC is operated in SPI mode. The interface needs, besides data lines, also a chip select and a card detect signal, which are implemented by two port pins. As an MMC socket does not have a card detect switch, the ground pin 6 of the MMC port is used as the card detect signal. The signal is directed onto the pin PTF3/PINT11, which is used as interrupt input. Pin PTM0 is used as chip select output. All signals are directed to the HICO.SH3 BASE.

SunDisk MMCs have the extended temperature range as a default! They automatically switch to sleep mode, if there was no command for longer than 5 ms. The power consumption is then only 50 μ A. The power consumption during operation is approximately 35 mA.

The advantage of an MMC compared to a CF card is the smaller size. The disadvantage is the serial data transfer. According to Hitachi measurement results, the data rate for the MMC is approximately 200 KByte/s compared to several Mbyte/s for a CF card.

2.4. Ethernet Controller

The Ethernet interface is constructed with the SMSC module LAN91C111.

The Ethernet controller is connected with a 16-bit data bus in area 2. The basic address of the module is fixed at 0x300 in this area via hardware. The bus interface is asynchronous; wait states are generated suitably via ARDY by the controller. To

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achieve the required timing behaviour of the LAN91C111 read and write, the signals are created in a PLD. For this, area 2 must be programmed for 3 wait states.

Besides the four data lines, the status signals Link and 10/100 Mbit are also directed to the HiCO.SH3 BASE to control the LEDs.

2.5. Display Connection

Only the eight lower data lines and seven control signals with 3.3 V level are directed to the HiCO.SH3 BASE from the internal LCD processor controller. This is sufficient for monochrome and simple colour displays with 256 colours.

For 5 V displays, the signals on the HiCO.SH3 BASE must be additionally directed via drivers. Additional supply voltages such as -25 V for monochrome LCD displays must also be created on the HiCO.SH3-BASE.

2.6. Touch Interface

An interface for a 4-conductor touch panel is implemented by the means of the analogue inputs AN4 and AN5, and the port pins PTJ3, PTJ4, and PTJ5.

Via the port pins, the supply voltage is connected to the x or y connectors of the touch panel. Via the analogue inputs AN4 and AN5, the voltage is measured in the x or y direction. The pen down recognition is implemented via interrupt over PINT10.

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The following allocation applies:

Status	PTJ5	PTJ4	PTJ3	AN4	AN5	PINT10
Read x value	0	0	0	X value	-	
Read y value	1	1	0	-	Y value	
Wait for Interrupt	1	0	1	-	-	Interrupt is activated
Wait Pen Up/Down	1	0	1	-	Read	

The four signals of the touch interface are directed to the HICO.SH3 BASE.

Caution:

After switching to wait, the pen down will only be recognized after a maximum of 300 ms, depending on the y coordinate.

2.7. I²C Bus

As interface for the real time clock and other modules, an I²C bus is implemented which is also directed to the HICO.SH3 BASE.

The bus is implemented by the means of the data bits 0 and 1 via an I/O port at the address 0xA8000040. Bit 0 is SCL and bit 1 is SDA. Writing 0 is being output, for writing 1 the line stays on high-impedance and is pulled up to high by a pull-up.

Via NMOSFETs, the bus is driven bi-directionally to the HICO.SH3 BASE. This enables the implementation of an I²C-Bus with a 5 V level to be implemented on the HICO.SH3 BASE. Pull-ups are required on the HICO.SH3 BASE!

2.8. Serial Interfaces COM2, COM3

With the module XR16L2750, two more serial interfaces are implemented on the HICO.SH3 CORE. The interfaces are basically compatible to 16550, but have 64-byte deep FIFOs. Both interfaces can directly drive IrDA transceivers by activating the IrDA mode of the interface by software.

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The lines TxD, RxD, RTS, and CTS are directed to the HiCO.SH3 BASE as TTL signals. The other handshake signals are not directed downwards, because no more pins are available on the connector.

COM3 is used as the internal connection to the AVR microcontroller and is also directed to the HiCO.SH3 BASE. For this, with the output signal DTR from COM3, the receiving line can be switched between the AVR and the HiCO.SH3 BASE. Sending always takes place to both participants.

For the reception, the following applies:

DTR, COM3	Interface
0	AVR
1	BASE

The DUART is supplied with a 3.684 MHz clock, from which the baud rates are derived. Compared to a PC, the baud rate is higher by the factor 2.

COM2 has the basic address 0xA8000080 and leads to the interrupt PINT2; COM3 has the basic address 0xA80000C0 and leads to PINT3.

2.9. GPIO

Via the three port pins PTM0, PTM1, and PTM2 of the processor, variants of the HiCO.SH3 CORE module are coded. For this, the pins are programmed as input with pull-up, and 0 Ω pull-down resistors are soldered to the outside.

Via a jumper, port pin PTG4 can be pulled to 0. With this, the bootloader part 2 can be activated.

The processor signal STATUS1 is directed to a green LED, the signal STATUS0 to a yellow LED. By the means of the LEDs, the current processor state can be identified.

Processor State	Green LED	Yellow LED
Reset	Off	Off

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Standby	On	Off
Sleep	Off	On
Normal	On	On

The signals STATUS0 and STATUS1 can also be programmed as port pins. The LEDs light up with the output of 0.

In addition, an Atmel (AVR) microcontroller ATMEGA8535L-8AI is used as a general purpose port interface. With this, a freely programmable, intelligent interface is implemented. The 15 port pins PA7.. PA0, BP0, PB1, PD7..PD4, and PD2 are directed to the HICO.SH3 BASE for free disposal. All pins can be programmed as digital input or digital output. Alternatively, the pins of port A can be operated as analogue inputs with 10-bit resolution and a voltage range of 0 .. 2.5 V. Alternatively, the pins of port D can be operated as PWM output, as interrupt input or as timer output. The pins PB0 and PB1 can be configured as counter inputs. In addition, the four port pins PC3..PC0 are directed to the HICO.SH3 BASE. They are primarily used to identify a BASE, but can be used differently.

The connection between the AVR and the SH3 takes place via the serial interface COM3. The AVR is clocked with 3.684 MHz. To receive data from the AVR, the DTR line of COM3 must be set to 1; the according bit in the UART will be programmed with 0.

The programming of the internal flash of the AVR can take place from the outside via the programmable plug, or from the SH3 via a local SPI interface. With this, a firmware download can be implemented via the bootloader of the SH3.

The SPI interface is implemented via a port at the address 0xa8000000. The data bits have the following meaning:

Bit	Meaning for Read	Meaning for Write
0	MISO	If SPI is enabled: SCK
1	Always 1	If SPI is enabled: RESET#
2	Always 1	If SPI is enabled: MOSI
3	Always 1	0 = SPI disabled 1 = SPI enabled
4..15	Always 1	-

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If SPI is enabled, the AVR can be reset by RESET# = 0 also without using the SPI interface.

The advantage of this solution is the high flexibility. Via the second microcontroller, besides simple analogue and digital I/Os also complex functions such as a keyboard decoder or a PS/2 interface can be implemented.

2.10. Bus Connection

The processor bus as well as the PCMCIA control signals is directed from area 5 to the HiCO.SH3 BASE. With this, on the HiCO.SH3 BASE the processor bus is available for fast extensions, and from the PCMCIA control signals, addresses and data an ISA bus can be created.

The processor bus has a 50 MHz Bus clock. This mean, that extensions via the processor bus have high demands on the electrical design of a base because of the high frequencies. The advantage is the possibility of connecting fast periphery with more performance. The data bus is fixed at 16-bit width. 8-bit modules are connected in a way that they are addressable at every other address.

The advantage of the ISA bus is mostly that a standard is offered in form of PC/104, which can be easily used for "rapid prototyping" or even for implementations in small series. Examples would be extensions by HiCO.CAN, HiCO.PCMCIA, or HiCO.MIO. The disadvantage of the ISA bus is the slow access rate of 1 μ s.

2.11. Reset

The hardware reset is activated by the voltage monitor with the integrated watchdog, TPS3305-18. The watchdog is not used!

Four different sources for a hardware reset are possible:

- Undervoltage at 3.3 V or 1.8 V supply
- Reset signal from the HiCO.SH3 BASE module
- Reset signal from the emulator connector
- Reset by port pin PTM3 of the processor

The reset by the port pin PTM3 takes place in a way that the bit in the port M control register is switched to "other function". After the reset, the pin is on input with pull-up. The switching immediately activates a reset.

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2.12. Voltage Supply, DC/DC Converter

The HiCO.SH3 CORE module received +3.3 V as primary supply voltage, which is used to additionally create the voltage of 1.8 V with a DC/DC converter on the module. As DC/DC converter, the module LTC3406B by Linear Technology is used. It comes with a 5-pin TSOP enclosure and manages with a very small SMD coil with 1210 design, because it clocks with 1.5 MHz. The maximum output current is 600 mA. The maximum power consumption is 0.5 A.

To supply the USB host interface, additional +5V are fed from the HICO.SH3 BASE.

The voltages +1.8 V and +3.3 V are monitored by the TI module TPS3305-18.

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3. HiCO.SH3 BASE Module

3.1. General

The HiCO.SH3 BASE board has a PC/104-compatible connection and is mechanically implemented accordingly. On the HiCO.SH3 BASE, several different extension functions are implemented, for which no room was found on the HiCO.SH3 CORE or which are not regarded as core functions.

3.2. Graphics Controller S1D13806

The BASE board has an additional graphics controller S1D138806. By the means of this graphics controller, also CRTs or larger LC displays can be controlled.

As LCD connector a 40-pin plug connector Hirose type DF13-40 is used. The pins are assigned in a way that VGA TFT displays with 18 bits can be directly connected via the existing flat conductor cable. At the remaining nine pins the signals of the touch controller, the analogue input ANA0, and the GPIO pins GPIO0 .. GPIO3 of the graphics controller are connected.

The signals for a CRT connection are directed to the HiCO.SH3 CON, where a standard HD-Sub15 jack is available.

The graphics controller is addressed in area 4; the registers are in the address range 0xB0000000 .. 0xB01FFFFFF; the frame buffer is in the range 0xB0200000 .. 0xB03FFFFFF.

Only the input CLKI1 has a clock; for the other two inputs CLKI2 and CLKI3 the frame ground connection is fixed. The bus clock is 50 MHz. The clock is created by a PLL ICS501, which is programmed via the port pins GPIO4 and GPIO5 of the VGA controller. For the clock the following applies, depending on the port pins:

GPIO5	GPIO4	Frequency
0	0	33 MHz
0	Z	Not permitted
0	1	41.25 MHz
Z	0	51.56 MHz
Z	Z	17 MHz

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Z	1	25.78 MHz
1	0	49.5 MHz
1	Z	24.75 MHz
1	1	66 MHz

The value 0 means that via the port pin the output is 0

The value Z means that the port pin is programmed for input

The value 1 means that via the port pin the output is 1

The port pins GPIO0, GPIO1, GPIO2, and GPIO3 of the VGA controller are directed to the TFT connection. They should be programmed as output and can, for example, be used to control the backlight.

At the port pins GPIO8, GPIO9, and GPIO10 of the VGA controller, pull-down resistors can be connected for identification purposes. For this, the pins must be programmed as inputs.

3.3. ISA Bus

The ISA bus has 16 data lines, 24 address lines and 15 control signals. The control signals are created with a PLD EPM7128S from the eight PCMCIA signals CE1A#, CE2A#, RD/WR#, ICIORD#, ICIOWR#, WAIT#, IOIS16#, and CKIO of the processor in area 5.

Within the 16 Mbyte large address range 0xB6000000 .. 0xB6FFFFFF, the memory signals MEMR# and MEMW# are output. Within the 1Mbyte large address range 0xB6000000 .. 0xB60FFFFF, SMEMR# and SMEMW# are also becoming active. Within the 1Mbyte large address range 0xB7000000 .. 0xB70FFFFFF, the I/O control signals IOR# and IOW# become active. From the I/O address range, the upper 512 Kbyte are internally used for the interrupt controller. This is no problem, as the I/O address range of x86 processors is only 64 Kbyte large.

Via three 8-bit latches type 74FCT373 and two 8-bit drivers type 74ABT245, the address and data lines of the processor SH7727 are connected to the ISA bus.

To achieve less signal switches on the ISA bus, the addresses are distributed via latches. After the access, the address stays on the ISA bus.

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The following timings are implemented:

Parameter	ISA Bus Specifications	HiCO.SH3
Command, 8-bit access	> 530 ns	536 ns
Command, 16-bit access	> 219 ns Memory > 154 ns I/O	175 ns 175 ns
Address set-up to command	> 91 ns	110 ns
Interval between commands	> 159 ns	160 ns
Address set-up to IOCS16#	< 91 ns	< 120 ns
Address set-up to MEMCS16#	< 66 ns	< 120 ns
Command to IOCHRDY, 8-bit access	< 362 ns	< 380 ns
Command to IOCHRDY, 16-bit access	< 59 ns	< 74 ns

Except for the command duration with 16-bit access, all timings are within the specifications of the ISA bus specification IEEE996. The shorter memory command is not regarded critical. In principle, the timings for 16-bit memory and I/O can be jointly extended to more than 219 ns.

3.4. Interrupt Encoder

Interrupt coding takes place in a PLD EPM7128S. In the PLD, the ISA bus interrupts are saved in two stages, with an interrupt request register and an interrupt service register. With this, edge-sensitive interrupts from the ISA bus are processed.

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The ISA bus interrupts produce the following IRL codes:

Interrupt	IRL Code	Priority
IRQ5	A	5
IRQ6	B	4
IRQ7	C	3
IRQ9	5	2
IRQ10	6	9
IRQ11	7	8
IRQ12	8	7
IRQ15	9	6

After the software has recognized them, interrupts must be released by a write access on an EOI port. The EOI port is addressed in the range 0x17080000 .. 0x170BFFFF at all even addresses. The number of the processed interrupt (5 .. 15) is written as value. The hardware ignores wrong values.

A mask register can block individual interrupts. The register is addressed by write access at all even addresses in the range 0x170C0000 – 0x170FFFFF. Writing of 1 blocks the according interrupt. After a reset, all interrupts are blocked.

For the allocation of the mask register, the following applies:

Bit	Interrupt
0	IRQ5
1	IRQ6
2	IRQ7
3	IRQ9
4	IRQ10
5	IRQ11
6	IRQ12
7	IRQ15

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3.5. Audio

The input and output signals of the Audio Codec of the HiCO.SH3 CORE are directed to a 10-pin post connector.

Furthermore, the microphone input and the left headset output are directed to the HiCO.SH3 CON module to enable the connection of a headset.

3.6. MMC Socket

As mass memory slot, a shielded socket is placed on the HiCO.SH3 BASE for an MMC.

The MMC socket is controlled by the SCI interface of the processor. As a MMC socket does not have a card detect switch, the ground pin 6 of the MMC socket is used as card detect signal. The signal is directed to pin PTF3/PINT11, which is used as interrupt input. Pin PTM0 is used as chip select output.

3.7. CF Connection

Due to space limitations, a Compact Flash socket is not planned for the BASE board. To make it possible to connect CF modules to the HiCO.SH3, all necessary signals are directed to a 50-pin connector. Via a flat conductor cable, an external board with a CF socket can be connected.

The control signals are generated by the PCMCIA controller of the SH7727 in area 6.

All output signals are driven by type 74LVT244 drivers. The supply voltage for the socket is 3.3 V and cannot be switched.

3.8. COM2, COM3

The eight COM2 and COM3 lines are directed via a type 74LVT244 driver to a post connector on the HiCO.SH3 BASE and to the HiCO.SH3 CON connector. The output signals are thus available with a LVTTTL level; the input signals are 5V tolerant.

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3.9. Connection for the Display SX09Q002

There is a connector on the HICO.SH3 BASE for the connection of Hitachi displays type SC09Q002 or SX09Q002.

The display contrast is controlled via the analogue output ANA0. A typical value for the DAC would be 0x90.

For the display SC009Q002-AZA, the brightness of the LED backlight is controlled via the analogue output ANA1. An operation amplifier with the factor 2, to achieve a maximum of 5 V output voltage, amplifies the ANA1 voltage. A typical value for the DAC would be 0x70.

3.10. Debug Interface

A 50-pin connector is placed on the bottom side of the HICO.SH3 BASE, to which the debug module SH4DBG can be connected.

The module includes a 10Mbit Ethernet interface based on the Ethernet controller CS8900 by Cirrus Logic, a RS232 transceiver, which is connected to COM2, eight LEDs, 63 Kbyte SDRAM and a PLCC socket for 64 Kbyte flash. After it has been connected, a bridge can be booted by the flash, which results in the switching off of the flash modules on the HICO.SH3 CORE module.

The debug interface is allocated to the following addresses in area 4:

Function Block	Data bus width	Address Range
Ethernet Controller	16 Bit	0xB0400300 .. 0xB040031E
SRAM	16 Bit	0xB0400400 .. 0xB040FFFE
Control Port	8 Bit	0xB0400200
LEDs	8 Bit	0xB0400202

The interrupt of the Ethernet controller is linked to the ISA bus interrupts. The Ethernet controller has the IRL code 4.

The flash module can only be addressed as boot memory in area 0. It cannot be operated in another area.

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Via the configuration bit 3 of the HiCO.SH3 BASE module, the debug board signals that it has been connected. 0 on bit 3 means that the board is connected.

Via bit 7 of the control port, the Ethernet controller can be switched into hardware standby mode. Bit 7 leads to the SLEEP# pin of the Ethernet controller; 0 activates the sleep mode, if the controller has been programmed accordingly. Via bit 6 of the control port, the RS232 transceiver is switched on and off; 0 switches the transceiver off. Bit 3 .. 0 of the control port are available as output bits. After a reset, all bits of the control port have the value 0.

Caution:

The Ethernet controller CS8900 requires 10 wait states for read access with 175 ns. The IOCHRDY of the Ethernet controller is not used.

3.11. Configuration Bits

Via four bits, several different configurations of the HiCO.SH3 BASE module can be signalled to the HiCO.SH3 CON module. The configuration bits are connected to the four port pins PC3..PC0 of the AVR controller on the HiCO.SH3 CON module.

Bit 3 is controlled by the debug board slot; the other three bits 0..2 are available. All bits are put on Vcc levels by pull-up resistors and can be grounded on the HiCO.SH3 BASE via 0 Ω resistors.

3.12. Voltage Supply

On the HiCO.SH3BASE, the voltage 3.3 V is created from +5 V from the ISA bus or from the supply voltage connector, with a DC/DC converter LM2651. The maximum output current is 1.5 A. This supplies the HiCO.SH3 BASE and the HiCO.SH3 CORE.

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4. HiCO.SH3 CON Module

The HiCO.SH3 CON module is connected from the HiCO.SH3 BASE, to simplify the joining of functions from the HiCOSH3 CON and the HiCO.SH3 BASE for customer-specific BASE modules.

A USB function and a headset connection are available.

In detail, the following connections are implemented:

COM1	RS232, D-Sub 9 connector
COM2	LVTTTL, 6-pin post
COM3	LVTTTL, 6-pin post
Headset	2.5 mm stereo jack plug
CRT	HD-Sub 15 jack
Fast Ethernet	RJ45 jack with link and traffic LED
USB function	
USB host	
Reset key	

The CRT and the USB connectors have protective circuits for electromagnetic compatibility.

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5. Debugging

The H-UDI interface of the processor is directed to a connector as emulator connector. The additional AUD interface (Advanced User Debugger) of the processor is not directed outwards, because with the use of the PCMCIA controller not all pins are available.

Currently no emulator is known which uses the AUD interface.
The Codescape emulator Dash3 works with HiCO.SH3 without any restrictions.

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