

HiCO.nect

**Design Guidelines
Connection of CORE with BASE boards**

**HiCO.nect.DOC
Manual**

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1	First edition	26.11.02/ Bue
2	Names changed Section 6.1 SDA5 and SCL4 on J1 exchanged Section 3 Data lines D[15 .. 0]	21.03.03/ Bue
3	Change to emtrion	07.07.03 / Bue
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1 Introduction

HiCO.nect is a plug definition for the connection of CPU modules, so-called CORE modules, with carrier boards, so-called BASE modules.

This document describes the three plug connectors and their allocation, and includes information to enable the development of new, pin-compatible modules. For this, the plugs and signals are described as follows:

Up to now, the pin definitions were used for CORE modules with Hitachi Super-H and ARM9 processors. It must be checked if an expansion to other processor types, such as XSCALE, or PowerPC is possible.

To remain open for other designs, a series of pins on the plugs J2 and J3 are reserved optionally. The plug allocation, section 6, shows these pins with grey shading. The white fields are defined as mandatory signals. If the allocation is done differently than specified, it must be observed that there are no signal conflicts with existing modules.

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2 Plug Connectors

The connection between the CORE and the BASE takes place via three plug connectors type Hirose FX6.

The signals of the processor bus and the supply voltages are directed via an 80-pin plug J1.

A series of input and output signals are directed via the two 50-pin plug connectors J2 and J3. On each plug, some pins are reserved for board-specific signals; the others are fixed.

On the CORE modules, a header type Hirose FX6-80P-0.8SV2 and two headers type Hirose FX6-50P-0.8SV2 are reserved.

On the carrier board, respective receptacles type Hirose FX6-80S-0.8SVx and FX6-50S-0.8SVx are reserved.

SVx stands for SV, SV1, or SV2. By choosing the receptacle type, the distance between the CORE and the carrier board can be fixed to 7 mm (SV), 8 mm (SV1), or 9 mm (SV2). All three receptacles must be of the same type.

Data sheet regarding the plug connectors can be found at: www.hirose.com

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3 Signal Characteristics

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	A[25 .. 0]	O	3.3	> 24	Processor address bus
J1	D[15 .. 0]	I/O	3.3	> 24	Processor data bus
J1	RD#	O	3.3	> 24	Read signal
J1	WR#	O	3.3	> 24	Write signal
J1	WE0#	O	3.3	> 24	Write enable 0 shows write access on low byte
J1	WE1#	O	3.3	> 24	Write enable 1 shows write access on high byte
J1	CLK	O	3.3	> 24	Bus signal pulse
J1	BS#	O	3.3	> 24	BS# shows the start of a bus cycle
J1	IRQ[3 .. 0]	IPU 10K	3.3	-	Interrupt inputs
J1	NMI	IPU 10K	3.3	-	NMI interrupt
J1	DRQ	I	3.3	-	DMA request
J1	DACK#	O	3.3	2	DMA acknowledge
J1	RDY/WAIT#	IPU 330R	3.3	-	Ready/Wait# Input
J1	CS[2 .. 0]#	O	3.3	2	Chip selects 2.. 0, CS0# is for boot prom
J1	RESI#	IPU 10K	3.3	-	Reset input
J1	RESO#	O	3.3	4	Reset output
J1	ID[3.. 0]	IPU	3.3	-	4-bit carrier board ID
J1	SCL5	I/O	5	-	PC bus SCL, 5 V-compatible, external pull-up 4k7 necessary
J1	SDA5	I/O	5	10	I ² C bus SDA, 5 V-compatible, external pull-up 4k7 necessary

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Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	BOOT8#	IPU 11K	3.3	-	BOOT8# switches data bus width for boot prom to 8-bit
J1	MD4	IPU 10K	3.3	-	Configuration bit MD4 from SH4
J2	ENAVEE	O	3.3	2	LCD, enable VEE
J2	ENAVDD	O	3.3	2	LCD, enable VDD
J2	M	O	3.3	2	LCS, AC signal for LCD display
J2	FLM	O	3.3	2	LCD, VSYNC
J2	DOFF#	O	3.3	2	LCS, display off, 0 = off
J2	CL1	O	3.3	2	LCD, HSYNC
J2	CL2	O	3.3	2	LCD pixel clock
J2	LCD[7 .. 0]	O	3.3	2	LCD, data bits [7 .. 0]
J2	REG#	O	3.3	2	PCMCIA, REG#
J2	VS1#, VS2#	I	3.3	-	PCMCIA, VS1#, VS2#
J2	CE1#, CE2#	O	3.3	2	CE1#, CE2#, CE2#
J2	RDY/BSY#	I	3.3	-	PCMCIA, RDY/BSY#
J2	RESET	O	3.3	2	PCMCIA, RESET
J2	BVD[2 ..1]	I	3.3	-	PCMCIA, BVD[2 ..] 1]
J2	CD[2 .. 1]#	I	3.3	-	PCMCIA, CD[2 ..] 1]#
J2	WAIT	IPU 10K	3.3	-	PCMCIA, WAIT
J2	IOIS16#	I	3.3	-	PCMCIA, IOIS16#
J2	IORD#	O	3.3	2	PCMCIA, IORD#
J2	IOWR#	O	3.3	2	PCMCIA, IOWR#
J2	PDRV#	O	3.3	2	Enable for PCMCIA signal driver
J2	I_CE1#	O	3.3	2	ISA Bus Interface, bus low enable

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Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J2	I_CE2#	O	3.3	2	ISA Bus Interface, bus high enable
J2	MMC_IRQ	IPU 10K	3.3	-	MMC, interrupt
J2	MMC_CS#	O	3.3	2	MMC, SPI mode chip select
J2	MMC_SCLK	O	3.3	2	MMC, SPI mode SCLK
J2	MMC_DO	I	3.3	-	MMC, SPI mode DO
J2	MMC_DI	O	3.3	2	MMC, SPI mode DI
J2	TOUCH_X1	A I/O	3.3	-	4-conductor touch controller, X1
J2	TOUCH_X2	A I/O	3.3	-	4-conductor touch controller, X2
J2	TOUCH_Y1	A I/O	3.3	-	4-conductor touch controller, Y1
J2	TOUCH_Y2	A I/O	3.3	-	4-conductor touch controller, Y2
J2	ANA[1 .. 0]	AO	3.3	5	Analogue outputs [1 .. 0], 0 .. + 3.3 V
J3	GPIO[14 .. 0]	I/O	3.3	-1.5/10	General Purpose I/O [14 .. 0]
J3	TXD#	O	RS232	2	COM1, TXD
J3	RXD#	I	RS232	-	COM1, RXD
J3	RTS	O	RS232	2	COM1, RTS
J3	CTS	I	RS232	-	COM1, CTS
J3	DTR#	O	RS232	2	COM1, DTR
J3	DCD	I	RS232	-	COM1, DCD
J3	TXD2	O	3.3	2	COM2, TXD
J3	RXD2	I	3.3	-	COM2, RXD
J3	RTS2	O	3.3	2	COM2, RTS
J3	CTS2	I	3.3	-	COM2, CTS
J3	TXD3	O	3.3	2	COM3, TXD

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Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	RXD3	I	3.3	-	COM3, RXD
J3	RTS3	O	3.3	2	COM3, RTS
J3	CTS3	I	3.3	-	COM3, CTS
J3	MIC	A I	-	-	Audio:, microphone input
J3	LINE_L	A I	-	-	Audio:, left line input
J3	LINE_R	A I	-	-	Audio:, right line input
J3	HEAD_L	A O	5	40	Audio, left head set output
J3	HEAD_R	A O	5	40	Audio, right head set output
J3	ETH_TDP	A O	-	-	Ethernet, transmit data positive
J3	ETH_TDM	A O	-	-	Ethernet, transmit data negative
J3	ETH_RDP	A I	-	-	Ethernet, receive data positive
J3	ETH_RDN	A I	-	-	Ethernet, receive data negative
J3	ETH_LED0#	O	3.3	10	Ethernet, link LED
J3	ETH_LED1#	O	3.3	10	Ethernet, 10/100 Mbit LED
J3	USBF_5V	I	5	-	USB Function, Vbus recognition
J3	USBF_PU	O	5	-	USB Function, full speed pull-up resistor
J3	USBF_DP	I/O	5	-	USB Function, data positive

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Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	USBF_DM	I/O	5	-	USB Function, data negative
J3	USBH_5V	O	5	500	USB Host, 5 V output
J3	USBH_DP	I/O	5	-	USB Host, data positive
J3	USBH_DM	I/O	5	-	USB Host, data negative
J1	BAT	-	3.0	10 μ A	3 V battery input
J1	VCC3	-	-	-	+ 3.3 V supply
J1	VCC5	-	-	-	+5 V supply, for USB
J1	GND	-	-	-	Ground
J3	AGND	-	-	-	Ground for audio signals

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4 AC Characteristics of the Signals

No specifications regarding the AC characteristics of the signals are available as yet.

The timing is determined by the used processors. For the processor SH-4 by RENESAS, the bus timing is adjustable through registers in a very flexible way; for the SH-3 by RENESAS processor it is fixed.

Whether the timing characteristics of the CORE and the carrier board match, must be determined for each individual case.

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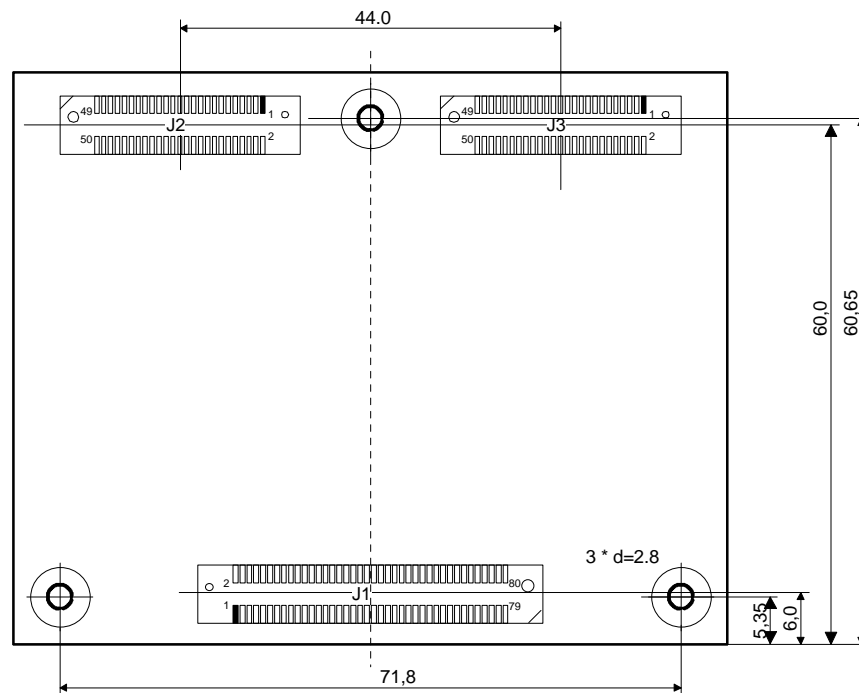
5 LCD Signal Color Table

Signal	SH7760-TFT	ARM9-TFT
LCD0	Blue1	Blue1
LCD1	Blue2	Blue2
LCD2	Blue3	Blue3
LCD3	Blue4	Blue4
LCD4	Blue5	Blue5
LCD5	Green0	Green0
LCD6	Green1	Green1
LCD7	Green2	Green2
GPIO0	Green3	Green3
GPIO1	Green4	Green4
GPIO2	Green5	Green5
GPIO3	Red1	Red1
GPIO4	Red2	Red2
GPIO5	Red3	Red3
GPIO6	Red4	Red4
GPIO7	Red5	Red5
GPIO8	N.A.	Blue0
GPIO9	N.A.	Red0

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6 Locations of Plug Connectors and Mounting Holes

The following diagram shows the locations of the plug connectors and mounting holes. The view is from the top to the CORE module or the carrier module. With a CORE module, the plug connectors are located at the bottom.



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7 Connector Assignments

7.1 J1

Type Hirose FX6, 80-pin

Pin	Signal	Pin	Signal
1	GND	2	VCC3
3	ID0	4	ID1
5	ID2	6	ID3
7	A0	8	A1
9	A2	10	A3
11	A4	12	A5
13	A6	14	A7
15	A8	16	A9
17	A10	18	A11
19	A12	20	A13
21	A14	22	A15
23	A16	24	A17
25	A18	26	A19
27	A20	28	A21
29	A22	30	A23
31	A24	32	A25
33	GND	34	VCC3
35	D0	36	D1
37	D2	38	D3
39	D4	40	D5

Pin	Signal	Pin	Signal
41	D6	42	D7
43	D8	44	D9
45	D10	46	D11
47	D12	48	D13
49	D14	50	D15
51	GND	52	VCC3
53	DRQ	54	CLK
55	DACK#	56	BS#
57	IRQ0	58	RD#
59	IRQ1	60	WR#
61	IRQ2	62	WE0#
63	IRQ3	64	WE1#
65	NMI	66	WAIT#
67	RESO#	68	CS2#
69	RESI#	70	CS1#
71	CS0#	72	GND
73	BOOT8#	74	SDA5
75	MD4	76	SCL5
77	BAT	78	VCC5
79	GND	80	VCC3

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7.2 J2

Type Hirose FX6, 50-pin

Pin	Signal	Pin	Signal
1	ENAVEE	2	GND
3	ENAVDD	4	REG#
5	DOFF#	6	VS1#
7	M	8	VS2#
9	FLM	10	RDY/BSY#
11	CL1	12	CE1#
13	CL2	14	CE2#
15	LCD0	16	RESET
17	LCD1	18	PDRV#
19	LCD2	20	BVD1
21	LCD3	22	BVD2
23	LCD4	24	CD1#
25	LCD5	26	CD2#
27	LCD6	28	WAIT#
29	LCD7	30	GND
31	GND	32	I_CE1#
33	ANA0	34	I_CE2#
35	ANA1	36	IOIS16#
37	GND	38	IORD#
39	MMC_IRQ	40	IOWR#
41	VCC3	42	GND
43	MMC_CS#	44	TOUCH_X1
45	MMC_SCLK	46	TOUCH_X2
47	MMC_DI	48	TOUCH_Y1
49	MMC_DO	50	TOUCH_Y2

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7.3 J3

Type Hirose FX6, 50-pin

Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO8
3	GPIO1	4	GPIO9
5	GPIO2	6	GPIO10
7	GPIO3	8	GPIO11
9	GPIO4	10	GPIO12
11	GPIO5	12	GPIO13
13	GPIO6	14	GPIO14
15	GPIO7	16	TXD2
17	GND	18	RXD2
19	TXD1#	20	RTS2
21	RXD1#	22	CTS2
23	RTS1#	24	TXD3
25	CTS1#	26	RXD3
27	DTR1#	28	RTS3
29	DCD1#	30	CTS3
31	ETH_LED0#	32	AGND
33	ETH_TDP	34	MIC
35	ETH_TDM	36	LINE_L
37	GND	38	LINE_R
39	ETH_RDP	40	HEAD_L
41	ETH_RDM	42	HEAD_R
43	ETH_LED1#	44	USBF_PU
45	USBH_5V	46	USBF_5V
47	USBH_DM	48	USBF_DM
49	USBH_DP	50	USBF_DP

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