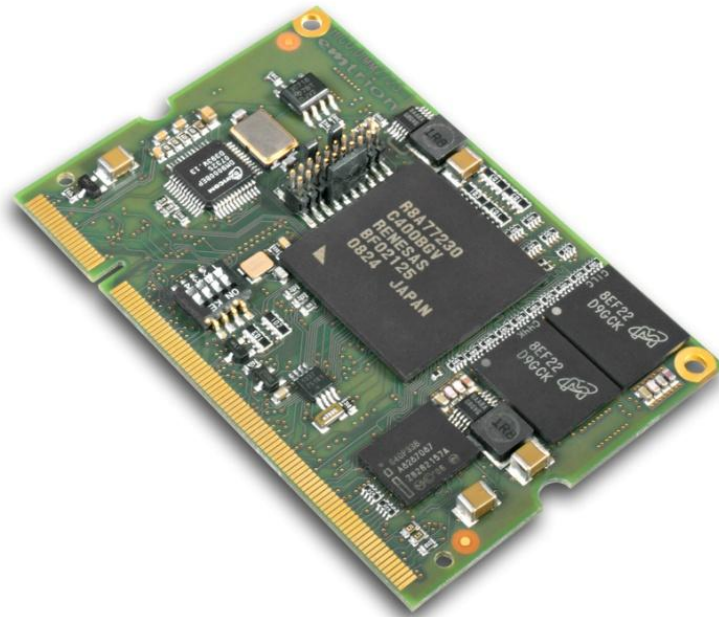


DIMM-SH7723

Processor Module with SH7723

Hardware Description

Rev6 / 24.02.2011



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Revision: **6 / 24.02.2011**

Rev	Date/Signature	Changes
1	11.11.2008/Sr	First revision
2	17.03.2009/Sr	Adaptations to Board-Revision R2A: <ul style="list-style-type: none"> - Chapter "General Purpose I/Os" added - Chapter "Timer Pulse Unit" added - WriteProtect-Function in chapter 4.2.1 added - Chapter 5.2: Signals at the pins 127-134 changed - Chapter 7.3.2 and 7.3.3 removed
3	07.01.2010/Sr	Adaptations to Board-Revision R3A: <ul style="list-style-type: none"> - Chapter 2: Block Diagram updated - Chapter 4.1.1 added - Chapter 4.20: TS Interface added - Chapter 4.21: address ranges corrected - Chapter 5.1: typo corrected: MEMD -> MPMD - Chapter 6.1 added - Chapter 6.2: Additional wiring information added - Chapter 6.3 added - Chapter 7.3.1: Dimensional Drawing updated
4	07.12.2010/Sr	Adaptations to Board-Revision R4A, R5A and R6A: <ul style="list-style-type: none"> - Productname changed from "HiCO.DIMM7723" to "DIMM-SH7723" - Chapter 2: new touch controller to block diagram added - Chapter 4.8: Expression "CCD camera" replaced by "CMOS camera" - Chapter 4.2.1: Description for new VPP pin for NOR-Flash write protection added - Chapter 4.9: New touch controller AR1020 added - Chapter 4.11: Processor allocations of SDHI interfaces added - Chapter 4.24: New reset source added (unstable RCLK) - Chapter 7.3.1: Drill diameter of mounting holes in dimensional drawing changed - Chapter 8: References [4] and [5] added - Design of the document changed

5	10.02.2011/Sr	- Chapter 4.6: Correction of addresses for USB Function - Chapter 7.3.1: Label of TS interface connector in dimensional drawing corrected
6	24.02.2011/Sr	- Chapter 7.3.1: Wrong drill diameter in dimensional drawing corrected

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1 Introduction

The DIMM-SH7723 processor module is a SODIMM sized CPU board based on the SuperH SH4A processor SH7723 from Renesas.

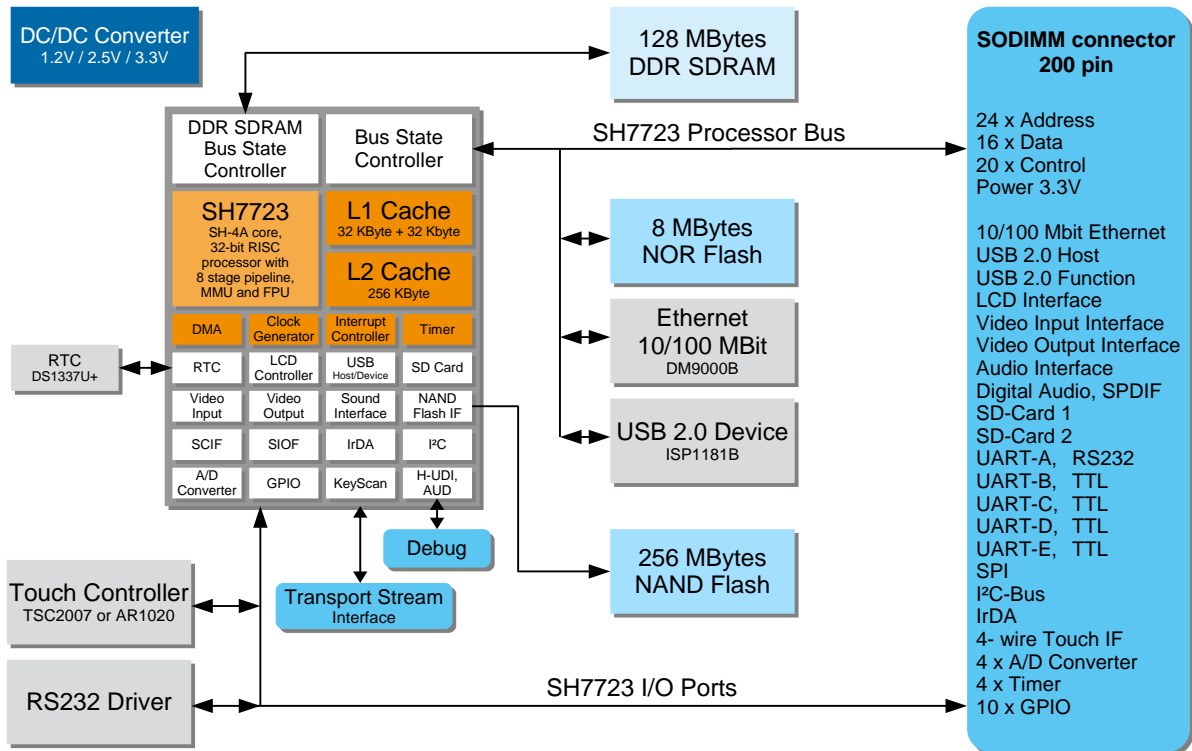
The processor core runs at 400 MHz and it includes a variety of functions required for multimedia applications. These include MPEG4 and H.264 accelerators, a 2D graphics accelerator, LCD controller, camera interface, and sound input/output module.

The module comes with 8 MB NOR-Flash, 256 MB NAND-Flash and 128 MB of DDR SDRAM. In addition to the processor and the memory, a 10/100-Mbps Ethernet controller, a USB Device controller and a touch controller are available.

All interfaces are accessible through the 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2.5 V keying.

The power consumption of the whole board is less than 1.5 W.

2 Block Diagram



3 Handling Precautions

Please read the following notes prior to installing the DIMM-SH7723 processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The DIMM-SH7723 does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The DIMM-SH7723 processor board uses the SuperH SH4A processor SH7723 from Renesas [1], a 32 bit RISC processor which runs at 400 MHz.

In addition to the CPU core with MMU, FPU and Caches, this processor provides a lot of features such as:

- Interrupt controller with 15 levels and nine external interrupt pins
- Bus state controller with SRAM, Burst ROM, SDRAM and PCMCIA interface
- NAND Flash controller
- 12-channel DMA controller with two external inputs
- Three 32 bit auto-reload timers
- Two SIOs with 64 byte FIFO
- Three UARTs with 16 byte FIFO and high speed mode
- Three UARTs with 64 byte FIFO and high speed mode
- I2C bus interface
- Video input module with camera capturing module and image processing unit
- Video output unit, digital outputs conform to ITU-R BT.601, ITU-R BT.656
- Video processing unit for MPEG-4 H.264 encoding and decoding
- LCD Controller for TFT displays up to SXGA and 24 bpp
- 2D graphic accelerator
- Sound interface with PCM and I2S format
- USB 2.0 Host with high-speed mode
- Two SD Card host controller
- 4-channel A/D converter
- H-UDI debug interface

Further details of the processor can be found in the SH7723 hardware manual [1].

4.1.1 Processor Clocks

The RCLK clock input of the CPU is supplied by a 32,768 kHz clock from the RTC chip and used as main clock. This clock is multiplied by the internal PLL to 400 MHz and then divided by various software configurable dividers.

The following table shows the configured internal clocks:

Clock	Frequency
CPU Clock ($I\phi$)	400 MHz
Memory Clock ($U\phi$)	133,3 MHz
SH Clock ($SH\phi$)	133,3 MHz
Bus Clock ($B\phi$)	66,66 MHz
SDRAM Clock ($B3\phi$)	133,3 MHz
Peripheral Clock ($P\phi$)	33,33 MHz

4.2 Flash

4.2.1 NOR-Flash

The DIMM-SH7723 contains 8 MByte NOR flash which serves for the bootloader. A flash memory PC28F640P33 from Intel is used and connected to the 16-bit wide data bus.

To use the write protect function the WP# Pin of the Flash device is connected to the processor GPIO PTT2. As default the signal is pulled down and the NOR Flash is protected.

Since DIMM-SH7723 Revision R4A also the VPP pin of the NOR-Flash can be controlled by a processor GPIO. This improves the write protection function. The VPP pin is connected via an inverter to the GPIO PTE5. As default the GPIO pin is pulled up.

The following table shows the protection mode according to the GPIO pin states of the CPU:

PTT2 [WP#]	PTE5 [VPP#]	write protection
0	0	Only locked blocks are write protected
0	1	All blocks write protected
1	0	No write protection
1	1	All blocks write protected

For further information to the write protection, please see the datasheet of the NOR-Flash [6].

The flash device is located in area 0 from 0x00000000 ... 0x007FFFFF.

4.2.2 NAND-Flash

To store the operating system and application data 256 MByte NAND-Flash are provided. A flash memory MT29F2G from Micron is used and connected to the eight bit NAND Flash controller of the processor.

To use the write protect function the WP# Pin of the Flash device is connected to the processor GPIO PTK7. As default the signal is pulled down and the NAND Flash is protected.

4.3 SDRAM

128 MByte DDR SDRAM are available as main memory. The memory consists of two 512 MBit DDR SDRAMs, type 8M*16*4, that are connected in parallel to a 32-bit wide data bus. They are clocked at 133 MHz and operate with CAS2.

As RAM devices two MT46V32M16BN-6 from Micron are used.

The RAM is located in area 2 and 3, in the address range 0x08000000 ... 0x0FFFFFFF.

4.4 Ethernet Controller

The Ethernet interface is driven by the DM9000B Ethernet controller from Davicom [2]. This controller comes with the Media Access Controller (MAC) and Physical Layer Interface (PHY) on a single chip.

A 16 Kbytes on-chip SRAM serves to buffer transmit- and receive frames. The chip is able to put itself to the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The Ethernet controller uses two addresses in area 5B of the processor. The index port is located at 0x16000000 and the data port at 0x16000002. The interrupt output of the Ethernet controller is connected to IRQ5.

The Ethernet signal lines as well as two status signals that serve to indicate the link status and the transfer speed are connected to the SODIMM connector. An appropriate 1:1 transformer must be added externally.

4.5 USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the internal host controller of the SH7723. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed-, full-speed and high-speed.

To switch the bus power, the control line USBH_PEN is connected via an inverter to the SODIMM connector. A logical "1" at the processor GPIO PTF5 switches the power on, a logical "0" turns the power off. The signal USBH_OC# reports an overcurrent at the GPIO PTF6 ("0" = overcurrent).

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally. The data lines are internally terminated with 15-K Ω pulldown resistors.

4.6 USB Function

The USB function port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The interface is realized with an ISP1181B USB peripheral controller from NXP [3]. The interface is USB 2.0 compliant, supporting data transfers at full-speed (12 Mbps).

The controller is addressed via two 16-bit registers, an address- and a data register that are located in area 5A, at the addresses 0x01400000 and 0x0140002. The controller is able to issue IRQ3 interrupts and to transfer data into the main memory via DMA channel 1.

The WAKEUP pin of the ISP1181B is connected to the pin GPIO PTF0 of the SH7723. Thus the power management of the interface can be controlled by the software.

The data lines and the control line VBUS are available at the SODIMM connector. External 15-K Ω pulldown resistors are not required.

4.7 Video Out & Graphic Display

The SH7723 includes an integrated LCD controller and a video output unit (VOU). Both interfaces use the same processor pins. This is why LCD and video out can't be used simultaneously.

4.7.1 Video Output

The video output unit (VOU) supports the video system NTSC with a maximum image size of 720 x 240 dots. The provided output interfaces are 16-bit Y/C interface or 8-bit multiplexed YC interface.

All data and control lines are available at the SODIMM connector.

A 27 MHz clock for the video output unit must be supplied from the base board.

4.7.2 Graphic Display

The LCD controller of the SH7723 can drive TFT displays with resolutions up to SXGA at 24bpp. The pixel clock for the display data is generated by an internal 64-bit pattern. Thus all timings can individually be adapted by software to the connected display.

All data and control lines are available at the SODIMM connector.

4.7.3 Video Destination

The signal VOU_DEST on the SODIMM connector is routed to the GPIO PTT3. It can be used to switch between different video destination on the base board, such as graphic display or a video codec. The signal VOU_RST# at GPIO PTE2 is provided to reset video codecs at the base board.

4.8 Video Input

The SH7723 comes with a video input unit (VIO) which can be used with different video sources, such as video codec or CMOS camera modules.

The interface at the DIMM-SH7723 is realised with an 8-bit data-bus available at the SODIMM connector and supports various input formats.

To switch between two video sources the signal VIO_SRC (GPIO PTT4) is available. To reset video codecs at the base board the signal VIO_RST (GPIO PTT5) can be used. Both signals are connected to the SODIMM connector

The clock for the VIO must be supplied from the base board.

4.9 Touch Interface

A 4-wire touch interface is implemented using a touch interface controller connected to the I²C bus interface of the SH7723.

During the further development and improvements the touch interface controller was changed with the board revision R4A. From revision R1A to R3A the TSC2007 from Texas Instruments [4] is used. The pen interrupt is connected to IRQ7. The 7-bit I²C-Address is 0x48. The AUX input of the TSC2007 remains unused.

Since revision R4A the AR1020 from Microchip [5] is used. The IRQ output of the controller is also connected to IRQ7 of the SH7723. The 7-bit I²C-Address is 0x4D.

The touch interface signals are available at the SODIMM connector.

4.10 Audio Interface, SSI port

The SH7723 processor has an integrated SIU (Sound Interface Unit) module that can be used to send and receive audio data from external audio codecs.

The Interface is connected to SODIMM connector, which allows the selection of an external audio codec. The input clock for the audio port must be externally supplied.

The SIU module also supports the SPDIF format. The input and output pins at the SODIMM connector have LVTTTL level and will need to be configured external according to the SPDIF specifications.

4.11 SD-Card Interface

The SH7723 includes two SD Card interfaces (SDHI0 / SDHI1) to drive memory- or I/O cards. The signals are routed with all necessary pull up resistors to the SODIMM connector.

The SDHI0 interface is connected to the first SD-Card interface on the SODIMM connector, and the SDHI1 is connected to the second interface.

4.12 Serial Ports

The DIMM-SH7723 comes with five serial ports which are all integrated in the processor SH7723. The SCIF modules have different sized FIFOs and up to two handshake signals.

At the SODIMM connector the interface names change to UART_A – UART_E.

An overview is shown as follows:

SH7723 interface	SODIMM name	handshake signals	FIFO size (byte)
SCIF1	UART_E	-	16
SCIF2	UART_D	-	16
SCIFA3	UART_A	RTS, CTS	64
SCIFA4	UART_C	-	64
SCIFA5	UART_B	-	64

All signals are available at the SODIMM connector. UART-A has been implemented as a RS232 port. The signal lines of UART-B to UART-E have LVTTTL level and will need to be configured by external drivers. RS232 adaptors, which can be plugged to a pin header, are available from emtrion.

4.13 IrDA Interface

The SH7723 has an on-chip IrDA interface which supports baud rates up to 115200 kBaud. The receive- and transmit-pins are routed to the SODIMM connector. The IrDA-transceiver must be added externally.

4.14 RTC DS1337

Since the integrated RTC of the processor SH7723 does not have a separate power supply the RTC DS1337 from Maxim is added. It is clocked by a 32.768 KHz crystal which also serves as clock source for the processor.

The DS1337 is connected to the I²C bus interface of the SH7723. The 7-bit I²C-Address is 0x68. An alarm interrupt is available on IRQ6.

Via the SODIMM connector the RTC can be buffered by an external battery. For timekeeping a supply voltage between 1.3 Volt and 3.3 Volt must be supplied. The current consumption is below 0.6 µA.

4.15 I²C- Bus

The SH7723 provides an I²C bus interface with transmission speeds up to 400 kb/s. The interface operates as a master.

Two devices are connected to the bus on DIMM-SH7723:

Slave	Device	Chip Address
Real Time Clock	DS1337U+	0x68
Touch Controller	R1A – R3A	TSC2007
	≥ R4A	AR1020

The bus connects to the SODIMM connector. The SCL and SDA lines are pulled up with 2.2 KΩ resistors to 3.3V.

4.16 SPI Interface

The MSIOF0 module of the SH7723 is configured as SPI interface. The four signals SPI_SCK, SPI_SS#, SPI_MOSI and SPI_MISO are available at the SODIMM connector.

4.17 Analog Inputs

The SH7723 contains a four channel A/D converter with a resolution of 10 bit. The maximum conversion time per channel is 15µs.

The analog inputs have a permissible input voltage range of 0V ... 3.3V and connected directly to the SODIMM connector.

4.18 General Purpose I/Os

Four portpins of the processor, which can be used as GPIOs, are routed to the SODIMM connector.

SIGNAL	SH7723 Port	Direction
GPIO_A	PTZ4	In/Out
GPIO_B	PTZ5	In/Out
GPIO_C	PTZ6	In/Out
GPIO_D	PTZ7	In/Out

4.19 Timer Pulse Unit

The four pins of the Timer Pulse Unit (TPU) of the SH7723 are routed to the SODIMM connector, too. They can be used as PWM or general purpose outputs.

SIGNAL	SH7723 Port	Direction
TPU0	PTG0	Output
TPU1	PTG1	Output
TPU2	PTG2	Output
TPU3	PTG3	Output

The TPU signals are multiplexed with the AUD signals in the processor. If a hardware debugger with AUD extension is used, the pins are not available as TPUs or GPIOs.

4.20 DIP Switches, TS-Interface, Status LED

Four DIP Switches can be read via the port pins PTX[3:0] of the SH7723. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0.

From board revision R3A the same port pins are used for the Transport Stream Interface. The four signals TS0_SCK, TS0_SDAT, TS0_SDEN and TS0_SPSYNC are available together with the I2C Interface at the connector J3. To use the Transport Stream Interface the two resistor networks RN1 and RN25 must not be soldered. Then the DIP Switches are out of function.

Please ask emtrion GmbH for a modified version of a DIMM-SH7723 module.

A bicolour LED is connected to the port pins PTJ7 and PTJ5 of the SH7723. If PTJ7 is high a green LED is lighting, if PTJ5 is high a red LED is lighting. If both ports are high both LEDs are on, which results in a yellow light.

4.21 Memory Map

The SH7723 processor provides 8 areas with 64 MB address space whose characteristics can be individually programmed. The address usage is as follows:

Area	Function	Bus Width	Address Region
0	8 Mbyte NOR-Flash	16-bit	00000000 – 007FFFFFFF
1	SH7723 intern	-	04000000 – 07FFFFFFF
2	lower 64 MByte DDR SDRAM	32-bit	08000000 – 0BFFFFFFF
3	higher 64 MByte DDR SDRAM	32-bit	0C000000 – 0FFFFFFF
4	SODIMM	8/16-bit	10000000 – 13FFFFFFF
5A	USB Device ISP1181	16-bit	14000000 – 15FFFFFFF
5B	Ethernet DM9000B	16-bit	16000000 – 17FFFFFFF
6A	SODIMM, CE2B#	8/16-bit	18000000 – 19FFFFFFF
6B	SODIMM, CE1B#	8/16-bit	1A000000 – 1BFFFFFFF
7	reserved	-	1C000000 – 1FFFFFFF

The timing characteristics of all areas but areas 4, 6A and 6B are programmed according to the requirements of the DIMM-SH7723 processor board.

Areas 4, 6A and 6B are reserved for external extensions and therefore configured with the slowest timing.

4.22 Interrupts

The processor SH7723 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor. Eight dedicated interrupt input pins are available for external devices.

Four interrupts lines are used for the USB Function, the touch controller, the Ethernet controller and the RTC. IRQ0 and IRQ1 are multiplexed with the sound interface and used for SPDIF. Therefore two normal interrupts and the NMI are available for external devices via the SODIMM connector.

The use of the interrupt inputs and the resulting interrupt code is displayed in the following table:

Name	Source	INTEVT
NMI	SODIMM	0x1C0
IRQ0	not available	-
IRQ1	not available	-
IRQ2	SODIMM (IRQ-B)	0x640
IRQ3	USB Host ISP1181	0x660
IRQ4	SODIMM (IRQ-A)	0x680
IRQ5	Ethernet controller DM9000B	0x6A0
IRQ6	DS1337	0x6C0
IRQ7	TSC2007	0x6E0

4.23 DMA

The SH7723 has two integrated DMA controller with 6 channels each.

Many integrated peripherals of the processor SH7723 like the Sound Unit, SD Card Controller, USB can be operated internally with DMA transfers.

Only channel 0 of each controller can receive external requests. This is used onboard for the USB Host ISP1181 (DREQ1).

There is no DMA channel available at the SODIMM connector.

4.24 Reset

There are several ways for issuing a reset signal:

- Two voltage monitors check the 3.3 Volt supply voltage of the board, the 1.2 Volt Core voltage of the processor and the 2.5 Volt DDR SDRAM voltage.
- Via the active low signal RESBASE# at the SODIMM connector
- Via the active low signal HRESI# at the Debug connector
- Via software by setting port pin PTF7 to 1
- Unstable RCLK clock (CPU main clock)

All resets are hardware resets of the whole board and issue a Power-on reset of the processor.

The duration of the reset signal is min. 140 ms. For resetting external devices the reset signal is available as an output at the SODIMM connector.

4.25 Debugging interface

At the 20 pole header J1 all signals of the User Debugging Interface H-UDI and also the additional six pins for emulator connection, AUD, are available.

Please contact emtrion for further details how to connect an emulator to J1.

4.26 Power Supply

A voltage of +3.3 volts, +/- 5%, @ max. 0.4 A must be supplied via the SODIMM connector. Further voltages for the processor and the other parts are generated on board.

4.27 HiCO.DIMM Interface

All interface signals of the board and an SRAM like bus interface for external peripheral additions are available at the SODIMM connector which is named HiCO.DIMM interface.

The HiCO.DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2.5V keying. These sockets are available from various manufacturers.

Usage details of the connector and its electrical and mechanical characteristics can be found later in this document.

Watch:

The pinout of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pinout may damage the DIMM-SH7723 and the carrier board.

Notes:

- The Video Output interface and the LCD interface share the pins 41 ... 76 of the SODIMM connector. Some of the pins change their behaviour and name according to the active interface.
 - Most of the pins are directly connected with the processor SH7723. For detailed electrical specification please refer to Section 44, Electrical Characteristics, in the SH7723 hardware manual [1]
-

5 Pin Assignments

5.1 J1, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	AUDCK	2	TCK
3	GND	4	GND
5	AUDSYNC	6	TRST#
7	+3.3 V	8	+3.3 V
9	AUDATA3	10	TDO
11	AUDATA2	10	ASEBRK#
13	AUDATA1	10	TMS
15	AUDATA0	10	TDI
17	GND	18	MPMD
19	HRESI#	20	RESET#

5.2 J12, DIMM connector

Type 200 pin SODIMM socket, 0.6 mm Pitch, 2,5V keying

Pin	Signal	Interface	Signal	Pin	
1	SPEED_LED#	Ethernet	USBH_PEN#	2	
3	ETH_TDP		USB Host	4	
5	ETH_TDM		USBH_DM	6	
7	GND		USBH_DP	8	
9	ETH_RDP		USB Device	USBF_VBUS	10
11	ETH_RDM			USBF_DM	12
13	LINK_LED#			USBF_DP	14
15	+3V3	Power		GND	16
17	n/c	UART	SCIF3_TXD#	18	
19	n/c		SCIF3_RXD#	20	
21	SCIF1_TXD		SCIF3_RTS#	22	
23	SCIF1_RXD		SCIF3_CTS#	24	
25	SCIF2_TXD	Touch	Touch_XP	26	
27	SCIF2_RXD		Touch_XM	28	
29	SCIF4_TXD		Touch_YP	30	
31	SCIF4_RXD		Touch_YM	32	

33	SCIF5_TXD	UART	A/D	ANA_IN 1	34		
35	SCIF5_RXD			ANA_IN 2	36		
37	ANA_IN4	A/D		ANA_IN 3	38		
39	+3V3	Power		GND	40		
41	LCD_D22	LCD, VOU		LCD_D23	42		
43	LCD_D20			LCD_D21	44		
45	LCD_D18			LCD_D19	46		
47	LCD_D16 / DV_HSYNC			LCD_D17 / DV_VSYNC	48		
49	LCD_D14 / DV_D14			LCD_D15 / DV_D15	50		
51	LCD_D12 / DV_D12			LCD_D13 / DV_D13	52		
53	LCD_D10 / DV_D10			LCD_D11 / DV_D11	54		
55	LCD_D8 / DV_D8			LCD_D9 / DV_D9	56		
57	LCD_D6 / DV_D6			LCD_D7 / DV_D7	58		
59	LCD_D4 / DV_D4			LCD_D5 / DV_D5	60		
61	LCD_D2 / DV_D2			LCD_D3 / DV_D3	62		
63	LCD_D0 / DV_D0			LCD_D1 / DV_D1	64		
65	+3V3			Power		GND	66
67	DV_CLKI			LCD, VOU		LCD_LCLK	68
69	LCD_DISP	LCD_DCK	70				
71	LCD_HSYN	LCD_DON	72				
73	LCD_VSYN / DV_CLKO	LCD_VCPWC	74				
75	VOU_DEST			LCD_VEPWC	76		
77	VOU_RST#	VIO		VIO_D7	78		
79	VIO_FLD			VIO_D6	80		
81	VIO_CKO**			VIO_D5	82		
83	VIO_CLK			VIO_D4	84		
85	VIO_HD			VIO_D3	86		
87	VIO_VD			VIO_D2	88		
89	VIO_SRC			VIO_D1	90		

91	VIO_RST#		VIO_D0	92	
93	+3V3	Power		GND	94
95	SDC2_D0	SDC2	SDC1	SDC1_D0	96
97	SDC2_D1			SDC1_D1	98
99	SDC2_D2			SDC1_D2	100
101	SDC2_D3			SDC1_D3	102
103	SDC2_CMD			SDC1_CMD	104
105	SDC2_CLK			SDC1_CLK	106
107	SDC2_CD#			SDC1_CD#	108
109	SDC2_WP#			SDC1_WP#	110
111	SPI_SS#			SPI	
113	SPI_SCK			SPI_MOSI	114
115	SCL	I2C	Audio	AUDIO_BCK	116
117	SDA			AUDIO_LRC	118
119	SPDIF_IN	SPDIF		AUDIO_DATI	120
121	SPDIF_OUT			AUDIO_DATO	122
123	GND	Power		AUDIO_MCLK	124
125	IrDA_IN#	GPIO		IrDA_OUT	126
127	AUD2 / TPU2***			AUD3 / TPU3***	128
129	AUD0 / TPU0***			AUD1 / TPU1***	130
131	GPIO_C			GPIO_D	132
133	GPIO_A			GPIO_B	134
135	+3V3	Power		GND	136
137	A22	Address A[23:0]		A23	138
139	A20			A21	140
141	A18			A19	142
143	A16			A17	144
145	A14			A15	146
147	A12			A13	148
149	A10			A11	150
151	A8			A9	152

153	A6		A7	154
155	A4		A5	156
157	A2		A3	158
159	A0		A1	160
161	+3V3	Power	GND	162
163	D14	Data D[15:0]	D15	164
165	D12		D13	166
167	D10		D11	168
169	D8		D9	170
171	D6		D7	172
173	D4		D5	174
175	D2		D3	176
177	D0		D1	178
179	CKIO	Bus Control	n/c	180
181	BS#**		n/c	182
183	RD#		IRQ4	184
185	RD/WR#		IRQ2**	186
187	WE0#		NMI	188
189	WE1#		RESO#	190
191	ICIORD#		RESI#	192
193	ICIOWR#		CE1B#	194
195	WAIT#		CE2B#	196
197	CS4#		IOIS16#	198
199	BAT		Power	GND

** The signals VIO_CKO, BS# and IRQ2 are multiplexed at the processor. As default IRQ2 is configured. To use VIO_CKO, R62 must be fitted and IRQ2 must be ignored from the software.

*** The AUD and TPU signals are multiplexed in the processor. The pins change their behaviour and name according to the active interface. The signals are available both at J1 and J2.

5.3 J3, Transport Stream Connector

Type 8-pin connector, Samtec FTS-104-01-F-DV

Pin	Signal	Pin	Signal
1	TS0_SCK	2	+3V3
3	TS0_SDAT	4	GND
5	TS0_SDEN	6	SCL
7	TS0_SPSYNC	8	SDA

Watch:

To use the Transport Stream Interface the two resistor networks RN1 and RN25 must not be soldered. Then the DIP Switches are out of function.

6 Signal Characteristics

Abbreviations:

AI analog input
 AO analog output
 A I/O analog bidirectional
 I digital input
 O digital output
 I/O digital bidirectional

PU xK x K Ω pullup resistor
 PD xK x K Ω pulldown resistor
 SR xR x Ω series resistor
 TIU xK transistor inverter with x K Ω pullup resistor
 TID xK transistor inverter with x K Ω pulldown resistor

6.1 J1, Debugging Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
Debug Interface					
TCK	I	PU 10K	3.3	-	JTAG clock input
TMS	I	PU 10K	3.3	-	JTAG mode select input
TRST#	I	PD10K	3.3	-	H-UDI reset input
TDI	I	PU 10K	3.3	-	Data input
TDO	O	-	3.3	2	Data output
ASEBRK#	IO	PU 10K	3.3	2	Pin for emulator
AUDSYNC, AUDCK, AUDATA[3:0]	O	-	3.3	2	Pins for emulator
MPDM	I	PU 10K	3.3	-	ASE mode input
Miscellaneous					
RESET#	O	-	3.3	1	Reset output
HRESI#	I	PU 10K	3.3	-	Reset input
+3V3	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

6.2 J2, SODIMM Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
Ethernet					
SPEED_LED#	O	-	3.3	4	100 MBit indicator
ETH_TDP	A O	-	-	-	TX diff. output pos.
ETH_TDM	A O	-	-	-	TX diff. output neg.
ETH_RDP	A I	-	-	-	RX diff. input pos.
ETH_RDN	A I	-	-	-	RX diff. input neg.
LINK_LED#	O	-	3.3	4	traffic indicator
USB Host					
USBH_PEN#	O	TIU 10K	3.3	4	Power enable for switch
USBH_OC#	I	-	3.3	-	Overcurrent from switch
USBH_DP	I/O	-	3.3	-	Diff. data positive
USBH_DM	I/O	-	3.3	-	Diff. data negative
USB Device					
USBF_VBUS	I	-	5	-	VBUS detection
USBF_DP	I/O	-	3.3	-	Diff. data positive
USBF_DM	I/O	-	3.3	-	Diff. data negative
UART					
SCIF1_TXD	O	PU 10K	3.3	2	transmit data
SCIF1_RXD	I	-	3.3	-	receive data
SCIF2_TXD	O	PU 10K	3.3	2	transmit data
SCIF2_RXD	I	-	3.3	-	receive data
SCIF3_TXD#	O	-	RS232	2	RS232 transmit data
SCIF3_RXD#	I	-	RS232	-	RS232 receive data
SCIF3_RTS#	O	-	RS232	2	RS232 modem control
SCIF3_CTS#	I	-	RS232	-	RS232 modem control
SCIF4_TXD	O	PU 10K	3.3	2	transmit data
SCIF4_RXD	I	-	3.3	-	receive data
SCIF5_TXD	O	PU 10K	3.3	2	transmit data
SCIF5_RXD	I	-	3.3	-	receive data
4-Wire Resistive Touch Interface					
TOUCH_XP	A I/O	-	3.3	-	X plus terminal
TOUCH_XM	A I/O	-	3.3	-	X minus terminal
TOUCH_YP	A I/O	-	3.3	-	Y plus terminal
TOUCH_YM	A I/O	-	3.3	-	Y minus terminal
Analog Input					
ANA_IN1	A I	-	3.3	-	10 bit analog input
ANA_IN2	A I	-	3.3	-	10 bit analog input

ANA_IN3	A I	-	3.3	-	10 bit analog input
ANA_IN4	A I	-	3.3	-	10 bit analog input
LCD/VOU (Video Output Unit)					
LCD_VCPWC	O	-	3.3	2	VCC power control
LCD_VEPWC	O	-	3.3	2	VEE power control
LCD_DON	O	-	3.3	2	LCD display enable signal
LCD_DISP	O	-	3.3	2	LCD display enable signal
LCD_VSYNC / DV_CLKO	O/O	-	3.3	2	LCD frame sync output VOU clock output
DV_CLKI	I	-	3.3	-	VOU clock input
LCD_HSYNC	O	-	3.3	2	LCD line sync output
LCD_DCK	O	-	3.3	2	LCD pixel clock output
LCD_LCLK	I	-	3.3	-	LCD source clock (external input)
LCD_D[23:18]	O	-	3.3	2	upper LCD colour data
LCD_D17 / DVI_VSYNC	O/O	-	3.3	2	LCD colour bit 19 / VOU frame sync output
LCD_D16 / DVI_HSYNC	O/O	-	3.3	2	LCD colour bit 18 / VOU line sync output
LCD_D[15:0] / DV_D[15:0]	O/O	-	3.3	2	lower LCD / Video output colour data
VOU_RST#	O	PU 10K	3.3	2	Reset signal for video device
VOU_DEST	O	PU 10K	3.3	2	Signal for selection of either video codec or LCD line drivers
VIO (Video Input Unit)					
VIO_D[7:0]	I	-	3.3	-	Video image input data
VIO_CLK	I	-	3.3	-	Video clock input
VIO_HD	I	-	3.3	-	Video hsync input
VIO_VD	I	-	3.3	-	Video vsync input
VIO_FLD	I	-	3.3	-	Field identification signal
VIO_CKO	O	-	3.3	2	Clock output
VIO_SRC	O	PD 47K	3.3	2	Selection of either camera or video codec input
VIO_RST#	O	TIU 47K	3.3	2	Reset signal for video device
SPI					
SPI_SS#	O	-	3.3	2	Slave select output
SPI_SCK	O	-	3.3	2	Clock output
SPI_MISO	I	-	3.3	-	Input data from slave
SPI_MOSI	O	-	3.3	2	Output data to slave
SD Card Interface					
SDC1_D[3:0]	I/O	PU 10K	3.3	2	SDC data
SDC1_CMD	I/O	PU 10K	3.3	2	CMD signal
SDC1_CLK	O	-	3.3	2	SDC Clock output

SDC1_CD#	I	PU 10K	3.3	-	Card detect input
SDC1_WP#	I	PU 10K	3.3	-	Write protect input
SDC2_D[3:0]	I/O	PU 10K	3.3	2	SDC data
SDC2_CMD	I/O	PU 10K	3.3	2	CMD signal
SDC2_CLK	O	-	3.3	2	SDC Clock output
SDC2_CD#	I	PU 10K	3.3	-	Card detect input
SDC2_WP#	I	PU 10K	3.3	-	Write protect input
I2C					
SCL	I/O	PU 2K2	3.3	-	I ² C clock signal
SDA	I/O	PU 2K2	3.3	-	I ² C data signal
Audio					
AUDIO_MCK	I	-	3.3	-	Master clock input
AUDIO_BCK	I/O	-	3.3	2	Sound bit clock
AUDIO_LRC	I	-	3.3	-	Sound L/R signal
AUDIO_DATI	I	-	3.3	-	Sound serial input data
AUDIO_DATO	O	-	3.3	2	Sound serial output data
SPDI	I	-	3.3	-	PCM input data
SPDO	O	-	3.3	2	PCM output data
IrDA Interface					
IrDA_OUT	O	-	3.3	2	transmit data
IrDA_IN#	I	-	3.3	-	receive data
Timer Pulse Unit					
TPU[3:0]	O	-	3.3	2	compare output / PWM output
General Purpose I/O					
GPIO[D:A]	I/O	-	3.3	2	digital input / output
Bus Interface					
A[23:0]	O	-	3.3	2	Processor address bus
D[15:0]	I/O	SR 82R	3.3	2	Processor data bus
CKIO	O	SR47R	3.3	2	66 MHz bus clock
WAIT#	I	PU 1K	3.3	-	Wait Input
BS#	O	PU 10K	3.3	2	start of a bus cycle
CS4#	O	-	3.3	2	Chip select output
RD#	O	SR 82R	3.3	2	Read signal
WE0#	O	SR 82R	3.3	2	Write access on even address
WE1#	O	-	3.3	2	Write access on odd address
RD/WR#	O	-	3.3	2	Data direction signal
IRQ4	I	PU 10K	3.3	-	Interrupt 4 input
IRQ2	I	PU 10K	3.3	-	Interrupt 2 input
NMI	I	PU 10K	3.3	-	NMI interrupt

RESI#	I	PU 10K	3.3	-	Reset input from carrier board
RESO#	O	-	3.3	1	Reset output to carrier board
ICIORD#	O	-	3.3	2	PCMCIA read signal
ICIOWR#	O	-	3.3	2	PCMCIA write signal
CE1B#	O	-	3.3	2	PCMCIA chip select for even addresses
CE2B#	O	-	3.3	2	PCMCIA chip select for odd addresses
IOIS16#	I	-	3.3	-	PCMCIA 16 bit signal
BAT	-	-	1.8 - 3.0	< 1 μ A	Battery backup input for RTC
+3.3 V	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

6.3 J3, Transport Stream Connector

Name	Direction	Add. wiring	Volt [V]	Current [mA]	Description
Transport Stream Interface					
TS0_SCK	I	PD 11K	3.3	-	Serial clock input
TS0_SDAT	I	PD 11K	3.3	-	Serial input of TS packet data
TS0_SDEN	I	PD 11K	3.3	-	Serial input enable
TS0_SPSYNC	I	PD 11K	3.3	-	Byte boundary signal pin
I2C Interface					
SCL	I/O	PU 2K2	3.3	-	I ² C clock signal
SDA	I/O	PU 2K2	3.3	-	I ² C data signal
Miscellaneous					
+3.3 V	-	-	-	-	+ 3.3 Volt supply
GND	-	-	-	-	Ground

7 Technical Characteristics

7.1 Electrical Specifications

Electrical Specification	
Supply Voltage	3.3 V, +/-5%
Current consumption	0.4 A max.

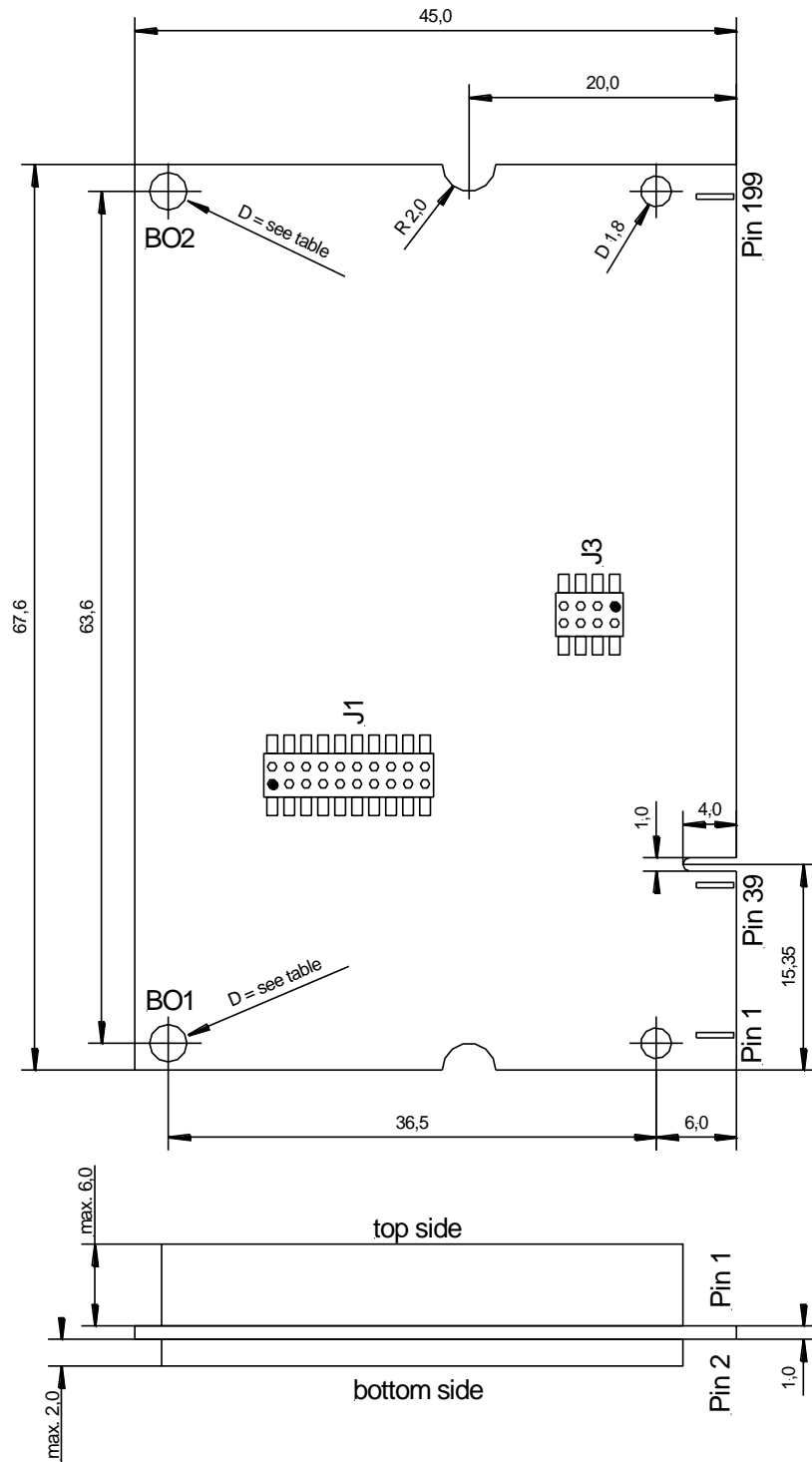
7.2 Environmental Specifications

Operating temperature	
Standard	0 ... +70°C
Extended	-40 ... +85°C
Storage temperature	
Storage temperature	-40 ... +125°C
Relative humidity	
Relative humidity	0 ... 95 %, non-condensing

7.3 Mechanical Specifications

Mechanical Specifications	
Weight	approx. 16 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 45.0 mm x 9.0 mm

7.3.1 Dimensional Drawing



The drill diameters of the two mounting holes BO1 and BO2 are changed with revision R6A:

Revision	Drill diameter
R1x to R5x	2,5mm
R6A and later	2,8mm

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