HiCO.SH7780-CORE

Processor Board with SH7780

HiCO.SH7780-CORE-DOC
Hardware Description

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1. Introduction

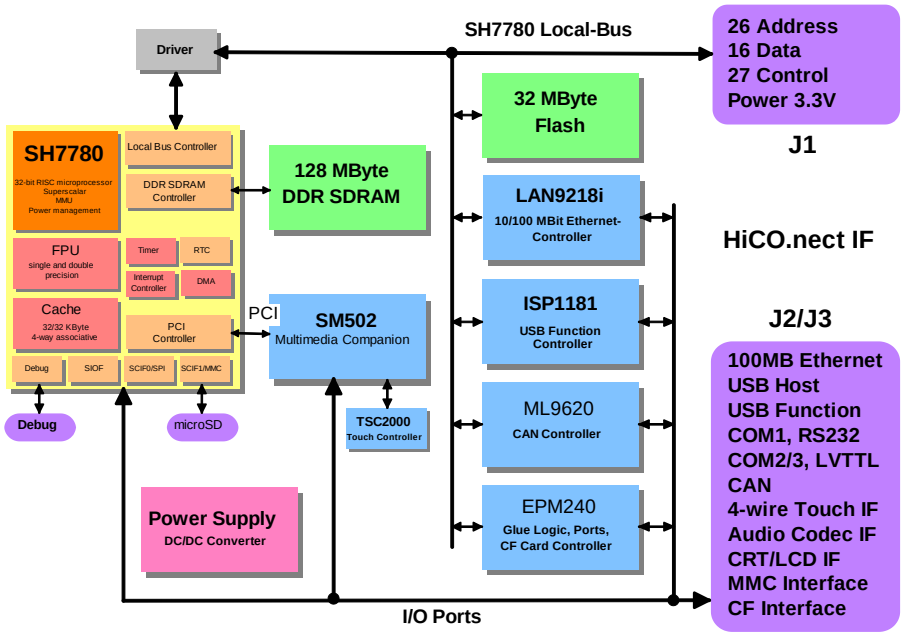
The HiCO.SH7780-CORE processor board is a CPU module based on the SuperH SH-4A processor SH7780 from Renesas. The board comes with 32 MB on-board-Flash and 128 MB of DDR SDRAM. In addition to the processor and memory, it is equipped with a Multimedia Companion Chip, a 10/100-Mbps Ethernet controller, an USB function controller and a CAN controller.

Most interfaces connect to the connectors on the carrier module, the so-called BASE. The connectors to the BASE comply with the HiCO.nect standard from emtrion. There is also an enlarged version with added local connectors available from emtrion as HiCO.SH7780-SBC.

Furthermore, the HiCO.SH7780-CORE processor board allows the installation of various standard operating systems such as Windows CE, Linux and QNX.

HiCO.SH7780-CORE only requires a +3.3V power supply to operate. The other voltages are generated on board.

2. Block Diagram



3. Before Installing the Module

Please read the following notes prior to installing the HiCO.SH7780-CORE processor module. They apply to all ESD (electrostatic discharge) components:

- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) a board, remove the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4. Functional Description

4.1. Processor

The HiCO.SH7780-CORE processor board uses the SuperH SH-4A processor SH7780 from Renesas [1], a 32–bit RISC processor which runs at 400 MHz.

In addition to the actual CPU core, this processor provides many features such as:

- Single and double precision FPU, IEEE754 compatible
- MMU with 4 GB of virtual address space
- 32-KB instruction cache and 32-KB operand cache, 4-way associative
- Interrupt controller with 15 levels
- Bus state controller with DDR-SDRAM interface
- PCI bus controller, according to PCI2.2
- Clock generator with power-down functions
- 12-channel DMA controller with two external inputs
- Four 32-bit auto-reload timers
- Two UARTs with 64 byte FIFO
- SSI and AC97 interfaces for Audio CODECs
- MMC controller
- H-UDI debug interface

The processor operates in the little endian mode, which allows you to make use of PC-compatible interfaces such as a CF card and operating systems like Windows CE.

The processor's input clock is 33 MHz. The internal PLLs are set to mode 1. This means that the processor runs at 396 MHz, the DDR SDRAMs are clocked with 158 MHz; the bus interface runs at 66 MHz and the internal peripherals at 33 MHz.

4.2. Address Map of Bus State Controller

The SH7780 processor provides 7 areas with 64 MB address space each at data widths from 8 – 32 bits. The address usage is as follows:

Area	Function	Bus Width	Address Region
0	32 Mbyte Flash	32/8-bit ***	00000000 – 01FFFFFF
	USB Device ISP1181	32-bit	02400000 – 02400004
	CAN controller ML9620	32-bit	02800000 – 0280003F
	Registers in PLD	32-bit	02C00000 – 02FFFFFF
	Ethernet LAN9218i	32-bit	03000000 – 033FFFFF
1	HiCO.nect interface area	16-bit	04000000 – 07FFFFFF
2	lower 64 MB DDR SDRAM	32-bit	08000000 – 0BFFFFFF
3	upper 64 MB DDR SDRAM	32-bit	0C000000 – 0FFFFFFF
4	PCI bus	32-bit	10000000 – 13FFFFFF
5	ISA bus interface area	8/16-bit	14000000 – 17FFFFFF
6	CF card interface area	8/16-bit	18000000 – 1BFFFFF

*** Enabling the BOOT8# signal allows you to boot from an external 8-bit PROM via HiCO.nect.

All Areas but area 1 are programmed according to the requirements of the HiCO.SH7780-CORE processor board. Area 1 is reserved for external extensions and therefore programmed with the slowest timing.

4.3. PCI Bus

The SH7780 processor provides a PCI bus Interface in area 4. This interface is used on board to connect the companion chip SM502 with the processor.

The bus is used 32 bit wide with 33 MHz clock. REQ1#, GNT1# are used for bus master accesses of the SM502. IDSEL is connected with AD16.

The PCI bus is not available outside the HiCO.SH7780-CORE.

4.4. HiCO.nect interface

Area 1 of the SH7780 processor is reserved for external hardware connected to the HiCO.nect interface of the HiCO.SH7780-CORE.

HiCO.nect is a standardized interface between the CPU boards from emtrion and BASE boards [2]. The interface consists of three connectors, one 80 pin connector J1 containing the processor bus interface and two 50 pin connectors J2 and J3 containing various peripheral signals.

The interface is an SRAM like asynchronous bus interface with 26 bit addresses, 16 bit data bus and control signals. Since this area is independent of all other functions of the HiCO.SH7780-CORE, the signal timing of the interface can be controlled by software and adapted to individual needs of external extensions.

Usage details of the connectors and their electrical and mechanical characteristics can be found later in this document.

4.5. Flash

32 MByte NOR flash memory is used as program memory. Two StrataFlash memories 28F128J3 are connected in parallel to a 32-bit wide data bus. The flash devices are located from 0x00000000 ... 0x01FFFFFF in area 0.

Signal BOOT8# on HiCO.nect's J1 connector serves to switch area 0 to an 8-bit wide data bus in order to boot from an external PROM. In this case, the on-board flash and the other devices of area 0 are switched to area 1.

4.6. RAM

128 MByte DDR SDRAM are provided as main memory. This RAM is located in the address range 0x08000000 … 0x0FFFFFFF which spans areas 2 and 3.

The memory consists of two 512 MBit DDR SDRAMs, type 8M*16*4, that are connected in parallel on a 32-bit wide data bus. They are clocked at 158 MHz, which means that they operate at 316 MHz using both clock slopes.

4.7. Multimedia Companion SM502

Many of the peripheral functions, especially the Graphic Controller, are integrated in the companion chip SM502GE08 from Silicon Motion [3].

This chip includes the Graphic Controller, USB Host, two serial ports, I^2C bus interface, SPI interface, two analog outputs and some GPIOs. The chip also has integrated 8 Mbyte SDRAM which is used as display memory and buffer for the USB host interface.

The SM502 is connected to the SH77780 via the PCI bus interface. REQ1# and GNT1# are used for bus master accesses. The interrupt is connected to INTA, IDSEL is connected to AD16. The PCI bus is clocked with 33 MHz.

4.8. Display Controller

The Display Controller is part of the SM502. It can drive displays with resolutions up to 1024 x 768 pixels at 24 bpp. With two different output interfaces analog CRTs and digital LCD displays can be used simultaneously. Both displays show the same picture.

TFT Displays and Colour STN Displays can be connected to the LCD output port. Monochrome STN displays are not supported.

The pixel clock for the display data is generated by an integrated PLL. Thus all timings can individually be adapted by software to the connected display.

The signals for a CRT are available on the 10 pin FFC connector J8. An external adapter with a female HD-Sub 15 connector is needed to connect a CRT.

The signals for LCDs are available at the connectors J2 and J3 of the HiCO.nect interface. Since only 16 data lines for the connection of a TFT display are available on the HiCO.nect interface, the least significant bits of Red and Blue are not available.

4.9. Touch Interface

Using the touch interface controller TSC2000 a 4 wire touch interface is implemented [7]. The touch controller is connected to the SPI interface of the SM502. The pen down interrupt is connected to GPIO_E0 of the SH7780 and causes interrupts with vector 0xF80. The level of the interrupt line can also be polled by software.

Besides the touch interface the TSC2000 can also measure the analog voltage input ANI1 of the HiCO.nect interface. This input has an input voltage range of 0 V … 2.5 V with a 100 Ω series resistor. The voltage is converted with 12 bit resolution.

The touch interface signals are available at the HiCO.nect connector J2.

4.10. USB Host

The USB Host is used to connect USB devices such as a keyboard, mouse, printer or a memory stick.

The USB host interface controller is also integrated into the SM502. It complies with the USB specification OHCI 1.0. Both low-speed- and full-speed data transfers are possible.

The VBUS power output is controlled via the LM3525 USB power switch with over-current protection. The switch is controlled by the two pins GPIO51 and GPIO52 of the SM502. A low level output at GPIO51 switches VBUS on. A low level input at GPIO52 signals an over current condition of the switch. The total power consumption of the connected USB devices should not exceed 0.5 A.

The lines are terminated with 15-KΩ pulldown resistors. They are connected to J3 of HiCO.nect.

4.11. USB Function

The USB function port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The interface is realized with an ISP1181B USB peripheral controller from NXP [4]. The interface is USB 2.0 compliant, supporting data transfers at full-speed (12 Mbps).

The controller is addressed via two 16-bit registers, an address- and a data register that are located in area 0, at the addresses 0x02400000 and 0x0240004. The controller is able to issue IRQ12 interrupts and to transfer data into the main memory via DMA channel 1.

The WAKEUP pin of the ISP1181B is connected to the pin GPIO_M1 of the SH7780. Thus the power management of the interface can be controlled by the software.

The data lines are connected to J3 of HiCO.nect.

4.12. Ethernet

The Ethernet interface is driven by the LAN9218i from SMSC [5]. This controller comes with the Media Access Controller (MAC) and Physical Layer Interface (PHY) on a single chip.

A 16 Kbytes on-chip SRAM serves to buffer transmit- and receive frames. The chip is able to put itself to the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The MAC and configuration data of the Ethernet controller are stored in a 93C46 type EEPROM.

The Ethernet controller is located in area 0 of the processor, in the address range 0x03000300 … 0x033FFFFF. A 32-bit wide data bus is used to optimize the performance. The interrupt output of the Ethernet controller is connected to IRQ0.

The data lines as well as two status signals that serve to indicate the link status and the transfer speed are connected to J3 of the HiCO.nect.

When using the Ethernet signals on an external BASE board, an appropriate 1:1 transformer or a Jack with integrated magnetics is required.

4.13. CAN Interface

The HiCO.SH7780-CORE also provides a full CAN interface according to CAN 2.0B. The interface is based on the CAN controller ML9620 from OKI [6].

The ML9620 is located in area 0 of the processor, in the address range 0x02800000 … 0x0280003F. Since the chip has only an 8 bit data bus the registers must be accessed at every fourth address. The interrupt output is connected to IRQ2.

The output data lines are connected to J3 of HiCO.nect as LVTTL signals. Note that an appropriate CAN transceiver has to be mounted on the BASE board.

4.14. Serial Ports

The SM502 has two integrated serial ports which are named UART-A and UART-B in this document. Both ports are 16C750 compatible with 64 Byte FIFOs. Only the two modem signals RTS and CTS are available in the UART function blocks. Since a DCD input is often used to detect a plugged cable the input GPIO53 of the SM502 serves as an additional DCD input for UART-A. This GPIO can be programmed to cause interrupts when the signal level of the DCD input changes.

The baud rate for the UARTs can be programmed based on 24 MHz input clock. Therefore baud rates up to 460 kBaud are possible.

The serial interface SCIF0 from the processor SH7780 is used as UART-C. This UART has also a 64 Byte FIFO and modem signals RTS and CTS. Additionally the baud rate clock signal is available at the HiCO.nect interface for synchronous operation.

UART-A has been implemented as a RS232 port on the HiCO.SH7780-CORE board. The data and modem signals are routed to J3 of the HiCO.nect interface.

The signal lines of UART-B and UART-C are connected directly to J3 of the HiCO.nect interface. The signals have LVTTL level and will need to be configured by external drivers.

4.15. Audio interface, SSI port

The SH7780 processor has an integrated SSI (Serial Sound Interface) module that can be used to send and receive audio data from external audio codecs. At lot of

data formats can be supported, including compressed and non-compressed data transfers.

The Interface is connected to HiCO.nect's J3 connector, which allows the selection of an external audio codec. The input clock for the audio port must be externally supplied.

4.16. I^2C Bus

The SM502 provides an I^2C bus interface with transmission speeds up to 400 kb/s. The interface operates as a master with 7-bit addressing according to the specification from Philips [8].

No device is connected to the bus on HiCO.SH7780-CORE.

The bus connects to J1 of the HiCO.nect plug connector via a bidirectional buffer PCA9515. At the external side of the I^2C bus no pull-up resistors are supplied. The user must add these resistors according to his individual needs.

4.17. MMC interface

The SH7780 includes a Multi Media Card interface that complies with the MMC specification, version 3.1. The interface is capable of transferring data at a speed of up to the half peripheral clock which is 16.5 MBaud. The port's command-, clock- and data line are connected to J2 of the HiCO.nect connector.

Additionally, a card detect input is realized via which an interrupt can be issued when plugging or removing a memory card. Inserting or removing a card will set a flip-flop that permanently issues the interrupt with vector 0xFC0 by using GPIO_K4 of the SH7780.

The actual state of the flip-flop and the state of the card detect pin itself can be read and at the address 0x02C00030.

The registers bits are defined as following:

Address	Bit 0	Bit 1
0x02c0 0030	0 = no interrupt	0 = socket is empty
	1 = interrupt is pending	1 = SDC is plugged

The flip-flop at bit 0 and thus the interrupt must be cleared by writing a 0 to that bit. The flip-flop will also be cleared by reset.

4.18. CF Card Interface

The bus state controller of the SH7780 processor is able to control the processor bus in the areas 5 and 6 in compliance with PCMCIA cards. The processor does not have a complete PC card controller. This is why a CompactFlash controller is implemented in a PLD.

The control signals of the CompactFlash controller are routed to the J2 connector of HiCO.nect via a driver 74LVT244. This allows an easy implementation of an interface on a BASE board.

The controller includes the following 4 registers

- Interface Status Register CF_ISR,
- General Control Register CF_GCR,
- Card Status Change Register CF_CSCR and
- Card Status Interrupt Enable Register CF_CSCIER.

The following applies:

Register	Access	Value After Reset	Address	Data Width
CF_ISR	R	-	0x02C00000	8 Bits
CF_GCR	R/W	0x00	0x02C00004	8 Bits
CF_CSCR	R/W	0x00	0x02C00008	8 Bits
CF_CSIER	R/W	0x00	0x02C0000C	8 Bits

The data region of the CompactFlash interface is located in area 6. The controller is able to issue interrupts via IRQ3 with interrupt vector 0x300. The timing of the interface is programmed according to the CompactFlash Specification 4.0 with 250 ns cycle time [9].

The controller is almost fully compatible with the PC card controller in the processor SH7727 from Renesas. For detailed information, please refer to section 30 of the SH7727 user manual.

4.19. RTC

The processor SH7780 includes an integrated RTC. The RTC is clocked by an 32.768 KHz crystal.

To keep the time the RTC is buffered by a CR1632 button cell battery with 3 Volt. The button cell is socketed in a battery holder and can be removed by the user when it is discharged. The battery's lifetime is more than 5 years.

4.20. Analog I/Os

HiCO.nect's J3 connector provides an analog input ANI1. The analog input signal is connected to the analog input AUX1 of the touch controller TSC200 as mentioned in chapter 4.9.

The analog input has a permissible input voltage range of 0 V … 2.5 V with a 100 Ω series resistor. The voltage is converted with 12 bit resolution.

J2 of the HiCO.nect interface also provides two analog outputs ANAO1 and ANAO2. These outputs are made from the two PWM outputs PWM0 and PWM2 of the SM502. Both output voltages can be individually set from 0 V to 3.3 V by use of two 12-bit counters, one for the low duration and one for the high duration. The outputs are filtered by 1st order low pass filters with 16 Hz.

After reset the output voltages are kept at 3.3 Volt. The short circuit output current is limited to 40 mA.

4.21. Digital I/Os

HiCO.nect's J3 connector provides 5 digital I/O pins. Within these the two pins GP13 and GP14 are driven by a PLD, GPIO8 and GPIO9 are driven by the pins

GPIO22 and GPIO23 of the SM502 and GP12 is connected with GPIO_H4 of the SH7780.

All these GPIOs are actually unused and reserved for future use.

The two pin header J9 is a high side switched 5 Volt output that is controlled by the pin GPIO57 of the SM502. If GPIO57 is set high, 5 Volt is driven at pin 1 of J9. If GPIO57 is low the voltage is off. J9 can be used as a switched power source for a backlight inverter.

The four ID pins at J1 of the HiCO.nect interface are connected to GPIO[19:16] of the SM502.

4.22. DIP switch, Status LED

The four way DIP switch SW1 is used by the Bootloader to select the start-up behaviour and the display mode. Actually the switches have the following meaning:

Switch	Position	Assignment
1 – 2 – 3	off – off – off	display type is ¼ VGA TFT, 320 x 240 pixel
	off – off – on	TBD
	off – on – off	Display type is SVGA TFT, 800 x 600 pixel
	off – on – on	TBD
	on – off – off	Display type is VGA TFT, 640 x 480 pixel
	on – off – on	TBD
	off – on – on	TBD
	on – on – on	TBD
4	on	Bootloader menu appears after reset
	off	Operating system is started after reset

A two colour LED is connected to pins GPIO_L0 and GPIO_L1 of the SH7780. GPIO_L0 drives the red LED and GPIO_L1 drives the green LED. The LEDs light if the I/O pin is low. After start-up this LED is used by the Bootloader to signal that the software is running.

4.23. Interrupts

The processor SH7780 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Nine special interrupt input pins are available for external devices and two GPIO pins are also used on HiCO.SH7780-CORE to generate interrupts.

Four pins, IRQ[7:4] can serve as a 4-bit IRL code. The interrupt controller decodes them to 16 different interrupts.

The use of the interrupt inputs and the resulting interrupt code is displayed in the following table:

Source	Pin	INTEVT
HiCO.nect interface	IRQ[7:4]	0x200 … 0x3C0
Ethernet LAN9218i	IRQ0	0x240
USB Device ISP1181	IRQ1	0x280
CAN controller ML9620	IRQ2	0x2C0
CF Card controller	IRQ3	0x300
Touch controller TSC2000	GPIO_E0	0xF80
MMC card detect	GPIO_K4	0xFC0
Companion chip SM502	PCI INTA	0xA20
NMI	NMI	0x1C0

The priority of the interrupt sources besides the NMI can be individually programmed.
The NMI input is not used on the HiCO.SH7780-CORE processor board. It may be used for external functions via the J1 connector of HiCO.nect.

4.24. DMA

Integrated peripherals of the processor SH7780 like the SSI module or the MMC controller can be operated internally with DMA transfers. Also the SM502 uses DMA for bus master transfers on the PCI bus.

Besides these the DMA channels 0 and 1 are available to external devices. DMA channel 0 is connected on board to the ISP1181 USB function controller. DMA channel 1 is connected to HiCO.nect's J1 connector and is thus available to external functions on the external BASE board.

4.25. Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks all supply voltages besides the +5V for the USB host and issues a reset when the respective supply voltage falls below its required level.
- The S1 momentary switch may be used to issue a manual reset.
- Via J1 of the HiCO.nect plug connector.
- Via the JTAG interface.
- Via any write access to address 0x02C00050.

All resets are hardware resets of the processor board issuing a hardware reset of the processor.

4.26. Debug interface

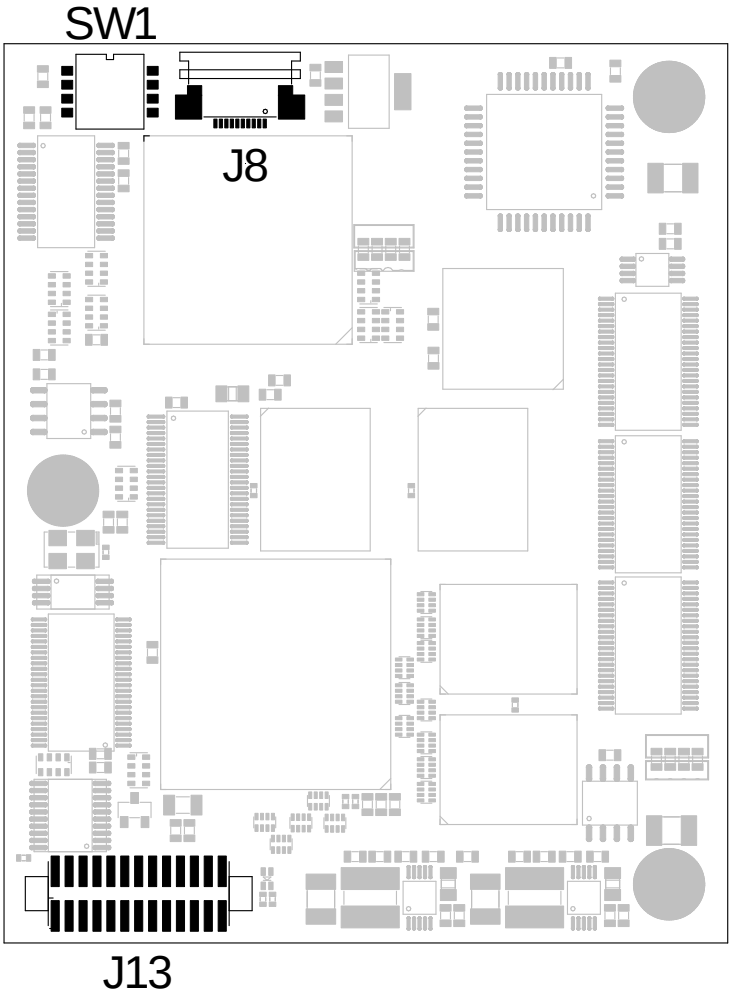
At the 26 pole header J13 all debug signals for H-UDI and AUD are available. Please contact emtrion for further details how to connect an emulator to J13.

4.27. Power Supply

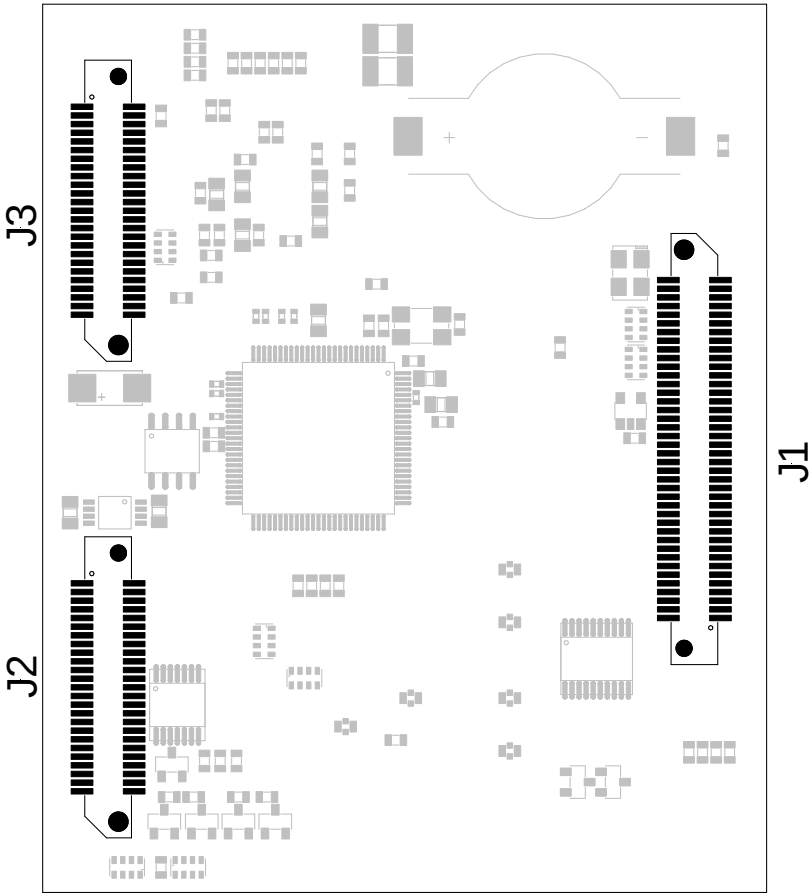
A voltage of +3.3 volts, +/- 5%, @ max. 1 A must be fed via J1 of the HiCO.nect interface. All further voltages for the processor and the other parts are generated on board by a DC/DC converter.

5. Location of the Connectors

Component side view HiCO.SH7780-CORE



Component side view HiCO.SH7780-CORE



6. Pin Assignments

6.1. J1, HiCO.nect

Watch:

At the HiCO.nect interface the pin1 location of connectors J1, J2 and J3 is different compared with pin 1 marking of Hirose. For clarification both pin counts are shown here.

Type Hirose FX6-80P, 80-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	**79**	GND	**2**	**80**	+3.3V
3	**77**	ID0	**4**	**78**	ID1
5	**75**	ID2	**6**	**76**	ID3
7	**73**	A0	**8**	**74**	A1
9	**71**	A2	**10**	**72**	A3
11	**69**	A4	**12**	**70**	A5
13	**67**	A6	**14**	**68**	A7
15	**65**	A8	**16**	**66**	A9
17	**63**	A10	**18**	**64**	A11
19	**61**	A12	**20**	**62**	A13
21	**59**	A14	**22**	**60**	A15
23	**57**	A16	**24**	**58**	A17
25	**55**	A18	**26**	**56**	A19
27	**53**	A20	**28**	**54**	A21
29	**51**	A22	**30**	**52**	A23
31	**49**	A24	**32**	**50**	A25
33	**47**	GND	**34**	**48**	+3.3V
35	**45**	D0	**36**	**46**	D1
37	**43**	D2	**38**	**44**	D3
39	**41**	D4	**40**	**42**	D5

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
41	**39**	D6	**42**	**40**	D7
43	**37**	D8	**44**	**38**	D9
45	**35**	D10	**46**	**36**	D11
47	**33**	D12	**48**	**34**	D13
49	**31**	D14	**50**	**32**	D15
51	**29**	GND	**52**	**30**	+3.3V
53	**27**	DREQ1	**54**	**28**	CKIO
55	**25**	DACK1#	**56**	**26**	BS#
57	**23**	IRQ4	**58**	**24**	RD#
59	**21**	IRQ5	**60**	**22**	WR#
61	**19**	IRQ6	**62**	**20**	WE0#
63	**17**	IRQ7	**64**	**18**	WE1#
65	**15**	NMI	**66**	**16**	WAIT#
67	**13**	RESO#	**68**	**14**	CS1#
69	**11**	RESI#	**70**	**12**	CS1#
71	**9**	EXTCS0#	**72**	**10**	GND
73	**7**	BOOT8#	**74**	**8**	SDA5
75	**5**	n/c	**76**	**6**	SCL5
77	**3**	BAT	**78**	**4**	VCC5
79	**1**	GND	**80**	**2**	+3.3V

6.2. J2, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	**49**	ENAVEE	**2**	**50**	GND
3	**47**	ENAVDD	**4**	**48**	REG#
5	**45**	DE	**6**	**46**	VS1#
7	**43**	DE	**8**	**44**	VS2#
9	**41**	FLM	**10**	**42**	RDY/BSY#
11	**39**	CL1	**12**	**40**	CE1#
13	**37**	CL2	**14**	**38**	CE2#
15	**35**	FP3	**16**	**36**	CFRESET
17	**33**	FP4	**18**	**34**	PDRV#
19	**31**	FP5	**20**	**32**	BVD1
21	**29**	FP6	**22**	**30**	BVD2
23	**27**	FP7	**24**	**28**	CD1#
25	**25**	FP10	**26**	**26**	CD2#
27	**23**	FP11	**28**	**24**	CFWAIT#
29	**21**	FP12	**30**	**22**	GND
31	**19**	GND	**32**	**20**	I_CE1#
33	**17**	ANAO1	**34**	**18**	I_CE2#
35	**15**	ANAO2	**36**	**16**	IOIS16#
37	**13**	GND	**38**	**14**	IORD#
39	**11**	MMC_IRQ	**40**	**12**	IOWR#
41	**9**	+3.3V	**42**	**10**	GND
43	**7**	n/c	**44**	**8**	TOUCH_X1
45	**5**	MMC_CLK	**46**	**6**	TOUCH_X2
47	**3**	MMC_DAT	**48**	**4**	TOUCH_Y1
49	**1**	MMC_CMD	**50**	**2**	TOUCH_Y2

6.3. J3, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	49	FP13	2	50	GP8
3	47	FP14	4	48	GP9
5	45	FP15	6	46	CAN_RX
7	43	FP19	8	44	CAN_TX
9	41	FP20	10	42	GP12
11	39	FP21	12	40	GP13
13	37	FP22	14	38	GP14
15	35	FP23	16	36	TXD2
17	33	GND	18	34	RXD2
19	31	TXD1#	20	32	RTS2
21	29	RXD1#	22	30	CTS2
23	27	RTS1#	24	28	TXD3
25	25	CTS1#	26	26	RXD3
27	23	n/c	28	24	RTS3
29	21	DCD1#	30	22	CTS3
31	19	ETH_100M#	32	20	GND
33	17	ETH_TDP	34	18	ANAI1
35	15	ETH_TDM	36	16	SSI_SCK
37	13	GND	38	14	SSI_WS
39	11	ETH_RDP	40	12	SSI_DAT
41	9	ETH_RDM	42	10	SSI_CLK
43	7	ETH_TRAF#	44	8	n/c
45	5	USBH_5V	46	6	USBF_5V
47	3	USBH_DM	48	4	USBF_DM
49	1	USBH_DP	50	2	USBF_DP

6.4. J13, Debug Connector

Type 26-pin connector, Samtec FTSH-126-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	+3.3 V	**2**	+3.3 V
3	TCK	**4**	GND
5	TRST#	**6**	MPMD#
7	TDI	**8**	TDO
9	ASEBRK#	**10**	RESO#
11	TMS	**12**	HRESI#
13	PLD_TDI	**14**	PLD_TDO
15	PLD_TCK	**16**	GND
17	n/c	**18**	n/c
19	n/c	**20**	n/c
21	AUD_SYN	**22**	AUD_D0
23	AUD_D1	**24**	AUD_D2
25	AUD_D3	**26**	AUD_CLK

6.5. J8, CRT Connector

Type 10-pin FFC, 0.5 mm pitch

Pin	Signal
1	CRT_RED
2	GND
3	CRT_GREEN
4	GND
5	CRT_BLUE
6	GND
7	CRT_HS
8	GND
9	CRT_VS
10	GND

7. HiCO.nect Signal Characteristics

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	A[25 .. 0]	O	3.3	> 24	Processor address bus
J1	D[15 .. 0]	I/O	3.3	> 24	Processor data bus
J1	RD#	O	3.3	> 24	Read signal
J1	WR#	O	3.3	> 24	Write signal
J1	WE0#	O	3.3	> 24	Write enable 0 shows write access on low byte
J1	WE1#	O	3.3	> 24	Write enable 1 shows write access on high byte
J1	CLK	O	3.3	> 24	Bus clock, 66 MHz
J1	BS#	O	3.3	> 24	BS# shows the start of a bus cycle
J1	IRQ[7 .. 4]	IPU 10K	3.3	-	Interrupt input code
J1	NMI	I	3.3	-	NMI interrupt
J1	DREQ1	IPU 10K	3.3	-	DMA request
J1	DACK1#	O	3.3	2	DMA acknowledge
J1	WAIT#	IPU 330R	3.3	-	Wait# Input
J1	CS1#	O	3.3	> 24	Chip select 1
J1	EXT_CS0#	O	3.3	2	Chip select 0 for external boot prom
J1	RESI#	IPU 10K	3.3	-	Reset input
J1	RESO#	O	3.3	4	Reset output
J1	ID[2.. 0]	IPU	3.3	-	3-bit BASE board ID
J1	SCL5	I/O	5	-	I^2C bus SCL, 5 V-compatible, external pull-up needed
J1	SDA5	I/O	5	-	I^2C bus SDA, 5 V-compatible, external pull-up needed

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	BOOT8#	IPU 10K	3.3	-	BOOT8# switches data bus width for ext. 8-bit boot PROM
J2	ENAVEE	O	3.3	2	LCD, enable VEE
J2	ENAVDD	O	3.3	2	LCD, enable VDD
J2	DE	O	3.3	2	LCD, DE signal for LCD display
J2	FLM	O	3.3	2	LCD, VSYNC
J2	CL1	O	3.3	2	LCD, HSYNC
J2	CL2	O	3.3	2	LCD pixel clock
J2	FP[23 .. 3]	O	3.3	2	LCD, data bits
J2	REG#	O	3.3	2	CF, REG#
J2	VS1#, VS2#	I	3.3	-	CF, VS1#, VS2#
J2	CE1#, CE2#	O	3.3	2	CF, CE1#, CE2#
J2	RDY/BSY#	I	3.3	-	CF, RDY/BSY#
J2	CF_RESET	O	3.3	2	CF, RESET
J2	BVD[2 ..1]	I	3.3	-	CF, BVD[2 ..] 1]
J2	CD[2 .. 1]#	IPU 10K	3.3	-	CF, CD[2 ..] 1]#
J2	CF_WAIT	IPU 10K	3.3	-	CF, WAIT
J2	IOIS16#	I	3.3	-	CF, IOIS16#
J2	IORD#	O	3.3	2	CF, IORD#
J2	IOWR#	O	3.3	2	CF, IOWR#
J2	PDRV#	O	3.3	2	CF driver enable
J2	I_CE1#	O	3.3	2	ISA Bus Interface, low enable

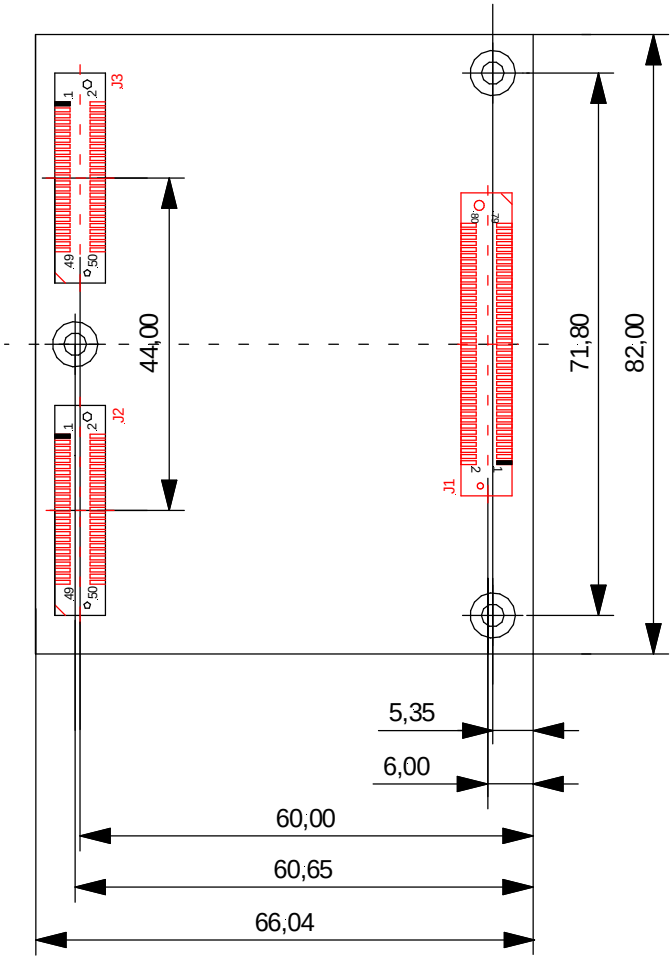
Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J2	I_CE2#	O	3.3	2	ISA Bus Interface, high enable
J2	MMC_IRQ	IPU 4K7	3.3	-	MMC, interrupt
J2	MMC_CLK	O	3.3	2	MMC, CLK
J2	MMC_DAT	I/O	3.3	-	MMC, DATA
J2	MMC_CMD	I/O	3.3	2	MMC, CMD
J2	TOUCH_X1	A I/O	3.3	-	4-wire touch, X min
J2	TOUCH_X2	A I/O	3.3	-	4-wire touch, X max
J2	TOUCH_Y1	A I/O	3.3	-	4-wire touch, Y min
J2	TOUCH_Y2	A I/O	3.3	-	4-wire touch, Y max
J2	ANA01	AO	3.3	40	Analog output, 0 ... +3.3 V
J2	ANA02	AO	3.3	40	Analog output, 0 ... +3.3 V
J3	GP[14 .. 8]	I/O	3.3	2	General Purpose I/Os
J3	TXD1#	O	RS232	2	COM1, TXD
J3	RXD1#	I	RS232	-	COM1, RXD
J3	RTS1#	O	RS232	2	COM1, RTS
J3	CTS1#	I	RS232	-	COM1, CTS
J3	DCD#	I	RS232	-	COM1, DCD
J3	TXD2	O	3.3	2	COM2, TXD
J3	RXD2	I	3.3	-	COM2, RXD
J3	RTS2	O	3.3	2	COM2, RTS
J3	CTS2	I	3.3	-	COM2, CTS
J3	TXD3	O	3.3	2	COM3, TXD

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	RXD3	I	3.3	-	COM3, RXD
J3	RTS3	O	3.3	2	COM3, RTS
J3	CTS3	I	3.3	-	COM3, CTS
J3	CAN_RX	I	3.3	-	CAN0 Receive
J3	CAN_TX	O	3.3	2	CAN0 Transmit
J3	ANAI1	A I	3.3	-	Analog input ANAI1
J3	SSI_SCK	I	3.3	-	SSI bit clock
J3	SSI_WS	I	3.3	-	SSI word select
J3	SSI_DAT	I/O	3.3	-	SSI data
J3	SSI_CLK	I	3.3	-	Oversampling audio clock
J3	ETH_TDP	A O	-	-	Ethernet, transmit data positive
J3	ETH_TDM	A O	-	-	Ethernet, transmit data negative
J3	ETH_RDP	A I	-	-	Ethernet, receive data positive
J3	ETH_RDN	A I	-	-	Ethernet, receive data negative
J3	ETH_TRAF#	O	3.3	10	Ethernet, Traffic LED
J3	ETH_100M#	O	3.3	10	Ethernet, 10/100 Mbit LED
J3	USBF_5V	I	5	-	USB Function, Vbus recognition

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	USBF_DP	I/O	5	-	USB Function, data positive
J3	USBF_DM	I/O	5	-	USB Function, data negative
J3	USBH_5V	O	5	500	USB Host, 5 V output
J3	USBH_DP	I/O	5	-	USB Host, data positive
J3	USBH_DM	I/O	5	-	USB Host, data negative
J1	BAT	-	3.0	10 µA	3 V battery input
J1	+3.3 V	-	-	-	+ 3.3 V supply
J1	VCC5	-	-	-	+5 V supply
J1	GND	-	-	-	Ground

8. Dimensional Drawing

Component side view; the solder side connectors are marked red.



9. Technical Data

9.1. Mechanical Data

Weight	60 g
Board	Glasepoxi FR-4, UL-listed, 12 layers
Dimensions	66 mm x 82 mm x 20 mm

9.2. Electrical Data

Supply voltage	3.3V, +/-5%
Power consumption	1 A max.

9.3. Environmental Conditions

Operating temperature **Storage temperature**	-20 ... +85°C, -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

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