



# HiCO.332

## Universal PC 104

### Process I/O Module

#### Processor Kernel

- 68332/G - 20 MHz
- 128KB Flash, sectored with bootstrap loader
- 128KB SRAM, can be buffered

#### Host PC Interface

- Plug-and-Play controller
- 8-bit PC/104 bus
- 2 KB DPM, with interrupt logic
- Capability of shared interrupts

#### Process Interfaces

- 1 x RS 485
- 2 x RS 232
- 8 binary inputs TTL level
- 8 binary inputs 24 VDC
- 8 binary outputs TTL level
- 8 binary outputs 24 VDC
- 8 analog inputs  $\pm 10V$  12 bits
- 2 analog outputs  $\pm 10V$  12 bits
- 2 encoder inputs, A/\*A, B/\*B, Z/\*Z or TTL each
- 10 TPU channels available



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## Processor kernel

The powerful 68332 is externally supplied with 32.768 kHz and runs internally with 20 MHz. The Flash has a size of 128K bytes and is divided into 5 sectors. The bootstrap loader in the first sector supports the loading of a firmware. For this, up to 96K bytes are provided. Two sectors of 8K bytes each are available for storing application data. The bootstrap loader supports deleting and writing these regions. The SRAM has a size of 128K bytes, is 16 bits wide and can be battery-buffered.

## Interface to the host PC

Thanks to the Plug-and-Play controller, several HiCO332s can be operated with one host PC, without having to change any jumper setting. The communication between the host PC and HiCO332 is handled via a 2 KB DPM. Semaphore instructions are supported by the hardware. This ensures consistency in the data via simple software mechanisms. The generation of interrupts on both sides is supported. The user may choose between PC-compatible interrupt signals and shared interrupt signals in accordance with the PC/104 specification.

## Serial interfaces

Altogether 3 serial interfaces are available. The 68332's SCI is build as RS485 interface. An external DUART provides two further interfaces which are implemented as RS 232.

## Binary I/O

16 binary inputs and 16 binary outputs are available. Eight IOs with TTL level are implemented for use as internal I/O (e.g. DIP switches and LEDs). Another 8 IOs are implemented with 24-VDC level to connect to the process.

## Analog I/O

HiCO332 provides 8 analog inputs and 2 analog outputs with a resolution of 12 bits each. ADC and DAC are connected to the QSPI. This frees the CPU32 from serving the analog channels; the conversion of input and output occurs cyclically in the background.

## Encoders and TPU channels

The TPU's first 6 channels are designed for use as encoder inputs for 2 two- or three-channel encoders. The TPU-internal FQD function provides two 16-bit wide counters. The remaining 10 TPU channels are available as TTL signals and can be used in accordance with the TPU-internal microcode (G type of the processor). This makes PWM signals, measurement of the frequency, counters, etc. available.

## Bootstrap loader

The integrated bootstrap loader ensures that the 68332's registers are set in accordance with the hardware. As a result, the developer can concentrate on the actual application and does not have to consider the hardware design. After the basic initialization of the 68332, the bootstrap loader first checks the bootstrap region with a checksum. After this, the remaining HW is initialized and the firmware area is examined by means of a checksum. If a checksum failure has occurred, the bootstrap loader switches to the receive mode for a new firmware. If no error has occurred, the program branches to the application firmware.



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**The bootstrap region provides the application firmware with several functions:**

<b>unsigned short BOOT_VERS (void)</b>
<i>This function determines the version of the bootstrap loader.</i>
_____
<b>int FW_LOAD (int source)</b>
<i>This function will load a firmware update. This is done in the S-Record format via one of the 3 serial interfaces or via the host PC's DPM. One utility for adding the checksum to an S-Record file and a utility for sending the S-Record file for the host PC are available.</i>
_____
<b>int FL_DELETE (word *start)</b>
<i>Deletes one of the two application data regions within the Flash.</i>
_____
<b>int FL_BL_WR (word *destination, word *source, lword wordcount)</b>
<i>Writes a data block to one of the two application data regions.</i>

## Firmware

To integrate the hardware functionality in the application firmware, two libraries are available. One library can be used in conjunction with any OS, the other one makes use of the VRTXMC real-time operating system from the Mentor Graphics company. The libraries were built with the Microtec C compiler and are available in this format. The source codes of the two libraries are available as well. The emtrion Tools section provides a wealth of emulators and debuggers for the support of development environments.

Please see the table below with respect to the technical data of the HiCO332. Customer-specific solutions relating to the hardware configuration (Flash, RAM, DPM, analog I/O) are also available.



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## Technical data HiCO332

Processor	68332 G type 20 MHz
Flash	2 x 8KB for application data, 96KB for application firmware, 16KB for bootstrap loader
RAM	128KB, can be buffered
DPM to the host PC	2KB with interrupt logic and semaphore support
Serial interfaces	1 x RS 485, 2 x RS 232
Binary inputs	8 with TTL level and 8 with 24 VDC level
Binary outputs	8 with TTL level and 8 with 24 VDC level
Analog inputs	8 with 12-bit resolution $\pm 10$ V
Analog outputs	2 with 12-bit resolution $\pm 10$ V
Encoder inputs	for 2 encoders; A/*A, B/*B, Z/*Z each
TPU I/O	10 (TTL level)
Supply voltage	+5 V, $\pm 15$ V
Power consumption	550 mA
Ambient temperature	0 °C to 70 °C
Storage temperature	-40 °C to +125 °C
Dimensions	PC/104 compatible

### Order codes:

HiCO.332-PC	PC/104 Process I/O module
HiCO.MIO-SW	Software for HiCO.332 with Samples
HiCO.332-SA	Stand Alone Process I/O module
HiCO.332-SW	Software/Firmware HiCO.332 (Source)



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