

HiCO.SH7760-CORE

Processor Board with SH7760

HiCO.SH7760-CORE-DOC
Hardware Description

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emtrion

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Revision History

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1	First edition	2004-04-20 / Bue
2	Connector J105 changed, new connector J95, range and impedance of the analog output corrected, name of the device changed to HiCO.SH7760-CORE	2004-09-20 / Bue
3	added information about W90 and W100	2004-11-30 / Bue
4	added chapter with HiCO.nect signal characteristics, added information about pin count of HiCO.nect connectors, hint according to 1.5V with revision S182	2005-05-04 / Bue
5	characteristics of CAN and OCOx signals added, characteristic of MMC_IRQ at J2 changed	2005-05-09 / Bue
6	in chapter 6 characteristic of ANI2 corrected, in chapter 3.12 type of CAN transceiver changed, in chapter 3.13 description of MMC interface changed, in chapter 3.22 information about DIP switches and status port added	2005-10-10 / Bue
7	Changes in chapter 3.24, 5.2 and 7 due to the new board revision HICO.SH7760-CORE-3. The core voltage 1.5V is always available at J2, pin 35. A 4K7 pull-up is added to MMC_IRQ. In chapter 5.8 pin number corrected.	2006-05-02 / Bue

8	HiCO.SH7760 manual was separated into two different manual for SBC and CORE	2006-10-25 / Bue
9	List of supported displays in chapter 4.22 updated	2007-10-18 / Bue

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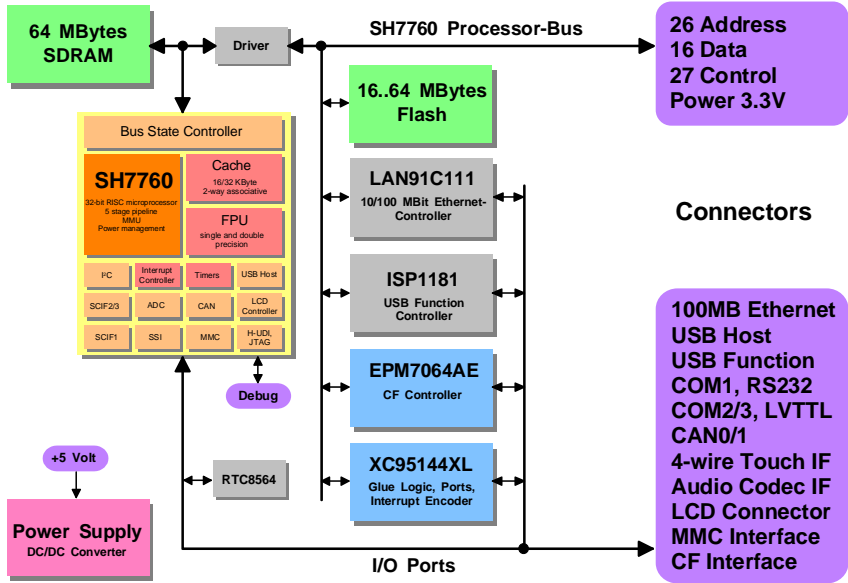
1 Introduction

The HiCO.SH7760-CORE processor board is a CPU module based on the SH7760 processor from Renesas. Depending on the version ordered, the HiCO.SH7760-CORE –CORE processor board comes with a 16 ... 64 MB on-board-Flash and 64 MB of SDRAM. In addition to the processor and memory, it is equipped with a 10/100-Mbps Ethernet controller and a USB function controller.

All interfaces are available at the connectors at the bottom side to the so-called BASE. The connectors to the BASE comply with the HiCO.nect standard from emtrion.

Furthermore, the HiCO.SH7760-CORE processor board allows the installation of various standard operating systems such as Windows CE, Linux and QNX.

2 Blockdiagramm



3 Before Installing the Module

Please read the following notes prior to installing the HiCO.SH7760-CORE processor module. They apply to all ESD (electrostatic discharge) components:

- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) a board, remove the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4 Functional Description

4.1 Processor

The HiCO.SH7760-CORE processor board uses the SH7760 processor type from Renesas [1], a 32-bit RISC SH4 family processor.

In addition to the actual CPU core, this processor provides many practical features such as:

- Single and double precision FPU, IEEE754 compatible
- MMU with 4 GB of virtual address space
- 16-KB instruction cache and 32-KB operand cache, 2-way associative
- Interrupt controller with 15 levels
- Bus state controller with programmable timing
- Clock generator with power-down functions
- 8-channel DMA controller with two external inputs
- 3 32-bit auto-reload timers
- 3 UARTs
- 2 SSI and AC97 interfaces for Audio CODECs
- 2 I²C bus channels
- MMC controller
- 2 CAN channels in accordance with CAN specification 2.0B
- SPI master/slave
- USB host according to USB 1.1
- LCD controller, max. 1024 * 1024 pixels, STN- and TFT displays
- 4-channel 10-bit AD converter
- H-UDI debug interface

The processor operates in the little endian mode, which allows you to make use of PC-compatible interfaces such as a CF card and operating systems like Windows CE.

The processor's input clock is 16 MHz. The internal PLLs are set to mode 3, according to the multipliers 12-4-2. This means that the processor runs at 192 MHz, the bus interface at 64 MHz and the internal peripherals at 32 MHz.

4.2 Bus Interface

The SH7760 processor provides 7 areas with 64 MB address space each at data widths from 8 – 32 bits. The address usage is as follows:

Area	Function	Bus Width	Address Region
0	16 ... 64 Mbyte Flash	32/8-bit ***	A0000000 – A3FFFFFF
1	On-board peripherals such as Ethernet, USB function, IO ports	16-bit	A4000000 – A7FFFFFF
2	External expansions	16-bit	A8000000 – ABFFFFFF
3	64 Mbyte SDRAM	32-bit	AC000000 – AFFFFFFF
4	External expansions	16-bit	B0000000 – B3FFFFFF
5	External expansions, e.g. ISA bus	8- / 16-bit	B4000000 – B7FFFFFF
6	PC card range	8-/ 16-bit	B8000000 – BBFFFFFF

*** Enabling the BOOT8# signal allows you to boot from an external 8-bit PROM via HiCO.nect.

Areas 0, 1, 3 and 6 were programmed according to the requirements of the HiCO.SH7760-CORE processor board. Areas 2, 4 and 5 were programmed with the slowest timing.

4.3 Interrupts

HiCO.SH7760-CORE comes with an interrupt encoder that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor as a 4-bit IRL code. For this, the processor's interrupt controller has to be programmed for level-encoded interrupt requests.

There are 7 local interrupt sources with these levels:

Source	Interrupt Level
Ethernet, LAN91C111	15
USB Function, ISP1181	12
CF Interface	9
Touch Pen Down/Up	6
MMC Card Detect Change	4
COM1, DCD Change	3
RTC	1

In addition, a 4-bit code can be applied by another external interrupt encoder via the J1 connector of the HiCO.nect plug connector. The codes are in accordance with the IRL coding of the processor's interrupt controller.

The following values are possible:

External Interrupt Code	Interrupt Level
0x1	14
0x2	13
0x4	11
0x5	10
0x7	8
0x8	7
0xA	5
0xD	2
0xF	No interrupt

The 7 levels of the local interrupts cannot be provided via HiCO.nect, they will be ignored.

All interrupts can be disabled via two 8-bit mask registers. The two registers are located at the addresses 0xa4000000 (low byte) and 0xa4000002 (high byte), respectively.

The following assignment applies:

Register	Data Bit	Meaning
0xa4000002	D[7..0] = IRQ[15..8]	1 = IRQ is disabled 0 = IRQ is enabled
0xa4000000	D[7..1] = IRQ[7..1] D0 = unused	1 = IRQ is disabled 0 = IRQ is enabled

All bits of both mask registers will be set to 1 upon reset. This means that all interrupts are disabled after a reset. The mask registers can be read back.

In addition to the normal interrupts, an NMI input is available. This input is not used on the HiCO.SH7760-CORE processor board. It may be used for external functions via the J1 connector of HiCO.nect.

4.4 DMA

The DMA channels 0 and 1 are available to external devices.

DMA channel 0 is connected to the ISP1181 USB function controller. DMA channel 1 is connected to HiCO.nect's J1 connector and is thus available to external functions on the external BASE board.

4.5 RAM

A 64-MB SDRAM is provided as main memory. This RAM is located in the address range 0xAC000000 through 0xAFFFFFFF in area 3.

The memory consists of two 256-Mbps RAMs, type 4M*16*4, and are operated in parallel on a 32-bit wide data bus. They are clocked at 64 MHz and run with CAS latency 2.

4.6 Flash

A 16 ... 64 MB flash memory may be used as program memory. The flash devices are located from 0xA0000000 ... 0xA3FFFFFF in area 0. Two StrataFlash memories in the BGA64 package are installed. Both flash memories are connected in parallel to a 32-wide data bus.

Signal BOOT8# on HiCO.nect's J1 connector serves to switch area 0 to an 8-bit wide data bus in order to boot from an external PROM. In this case, the on-board flash devices are disabled.

4.7 Serial Ports COM1 ... COM3

The SH7760 processor has three serial ports with integrated FIFO, SCIF0, SCIF1 and SCIF2. All ports may be operated both asynchronously and synchronously. The ports SCIF1 and SCIF2 provide the handshake lines RTS and CTS.

The lines of port SCIF0 and SCIF1 are connected to J3 of the HiCO.nect plug connector and will need to be configured by external drivers.

The connection is as follows:

Processor Port	HiCO.nect Port
SCIF0	COM3: RXD, TXD
SCIF1	COM2: RXD, TXD, RTS, CTS

SCIF2 has been implemented as a complete RS232 port COM1 on the processor board. Using additional logic, the handshake signals DCD and DTR can be provided for this port; there are no DSR and RI signals. All signals are routed to J3 of the HiCO.nect plug connector.

The DCD input signal serves to indicate when a cable has been plugged. The line's level can be read on data bit D0 at address 0xA4000080. At each level change, a flip-flop is set and a level 3 interrupt will be permanently issued. The state of the flip-flop can be read and written to data bit D0 at 0xA4000088. The flip-flop and thus the interrupt will be cleared by writing a 0. The flip-flop will be cleared after reset.

The DTR output signal is selected by writing data bit D0 on address 0xA8000090. The state of the DTR signal can be read back to bit 0 on the same address.

The following applies for the two handshake signals DCD and DTR:

Signal	Address	Direction	Data Bus
DCD	0xA4000080	read/write	Bit[7..1] = unused Bit 0 = DCD
Delta DCD	0xA4000088	read/write	Bit[7..1] = unused Bit 0 = Delta DCD
DTR	0xA4000090	read/write	Bit[7..1] = unused Bit 0 = DTR

4.8 I²C Bus

The SH7760 processor provides two I²C buses controllers according to Philips specification.

Bus 0 is used to select the real-time clock RTC8564 and the I²C digital potentiometer AD5241 [3].

Bus 1 connects to J1 (5V-compatible) of the HiCO.nect plug connector via bidirectional buffers. The pull-up resistors of the 5V side of bus 1 connects to the +5V USB power supply.

4.9 SSI Ports

The SH7760 processor has two SSI channels and one AC97 interface (HAC) for the selection of external audio codecs.

Interface SSI0 is connected to HiCO.nect's J3 connector, which allows the selection of an external audio codec. Also, the input clock for the port must be externally supplied.

The SSI1 port is not used.

4.10 USB Host

The SH7760 processor has a USB host controller that complies with the USB 1.0 specification. Here, USB devices such as a keyboard, mouse, printer or a memory stick can be connected.

Both low-speed- and full-speed data transfers are possible. The lines are terminated with 15-K Ω resistors against GND. Power is supplied via the LM3525 single port USB power switch with over-current protection. The total power consumption of all connected USB devices should not exceed 0.5 A.

4.11 USB Function

The ISP1181 USB interface device [4] is a USB 1.0 compliant full-speed Interface (12 Mbps) and used as USB function controller. The USB function port allows the transmission of data to an external host, e.g. between a host PC and Windows CE via Active Sync.

The USB device is selected via two 16-bit registers, an address- and a data register located in the address region 0xA4000200 through 0xA40002FF. The controller is able to issue a level 12 interrupt and to transfer data into the main memory via DMA channel 0.

4.12 CAN Interface

The SH7760 processor provides two full CAN controllers according to CAN 2.0B.

The data lines of both channels and the error input of channel 1 are connected to J3 of HiCO.nect. Note that an appropriate CAN transceiver has to be mounted on the BASE board.

4.13 MMC Port

The SPI interface of the SH7760 processor is used to control a MMC. The interface is capable of transferring data at a speed of up to 4 MBaud. The SPI port's chip select-, clock- and data lines are connected to J2 of the HiCO.nect connector.

Additionally, a card detect input is available via which a level 4 interrupt can be issued when plugging or removing an MMC. Inserting or removing an MMC will set a flip-flop that permanently issues the interrupt.

The state of the flip-flop can be read and written to data bit D0 at address 0xA4000100. The flip-flop and thus the interrupt will be cleared by writing a 0. The flip-flop will be cleared after reset.

4.14 LCD Controller

The processor comes with a built-in LCD controller for using flat screens. The input clock for the controller can be selected between a 64-MHz bus clock, a 32-MHz peripheral clock and 25 MHz, which are supplied externally. The LCD controller's output signals are connected to the connectors J2 and J3 of HiCO.nect.

The upper 8 bits of the LCD controller on the HiCO.nect connector are connected to the pins GPIO[7 ... 0] of J2. Thus 16 data lines for the connection of a TFT display are available on an expansion module. Since the LCD controller only has 16 data lines, the colours red and blue are driven with 5 bits, the least significant bit 0 is not available. For the colour green all 6 bits are available.

If the upper 8 data lines are not needed, e.g. when using an STN display, they may also be programmed and used as GPIO port D.

4.15 Touch Interface

Using the SH7760's 2 analog inputs AN0 and AN1 and the port pins Port B[3 ... 1], a 4-wire touch interface is implemented. Port pin B4 is an input for reading the Pen Down signal; port pins B3, B2 and B1 are outputs used to control the touch interface.

Pen Down issues a level 6 interrupt. Pen Up must be identified by polling port B4.

The lines of the touch interface are connected to J2 of HiCO.nect.

4.16 RTC

The processor does not come with a built-in real-time clock. This is why the RTC5864 device is used.

The RTC5864 device connects to the I²C bus 0 and able to issue a level 1 interrupt. The clock is buffered by a CR2016 button cell.

4.17 Analog Input

HiCO.nect's J3 connector provides an analog input ANI2. The analog input signal is connected to the analog input AN2 of the SH7760 processor via a voltage follower. The permissible input voltage range is 0 to 3.3 volts. The voltage follower is operated with the supply VCC5 which must be available when using this input.

The analog inputs AN0 and AN2 are used for the touch interface, the analog input AN3 is not used.

4.18 Analog Output

J2 of the HiCO.nect plug connector provides the analog output CONT. This output can be used to drive a voltage (by software) from 0 V to 3.3 V by means of the AD5241 I²C digital potentiometer [3].

After power-on, the potentiometer is always in its middle position; the output voltage is 1.65 V. The output impedance is 4.7 K Ω at 3.3 V and 104.7 K Ω at 0 V, respectively.

The voltage is normally used for contrast control of LCD displays.

4.19 Digital Outputs

HiCO.nect's J3 connector provides 8 digital I/O pins. The pins may either be programmed as output data D8 ... D15 of the LCD controller or as GPIO port D.

The processor pins are directly connected to J3. If you wish to use these pins, we recommend that you connect suitable drivers with a 3.3V supply voltage to the lines.

Furthermore, there are 2 outputs OCO1# and OCO2#. They are selected via the AD5241 I²C digital potentiometer [3]. The maximum current of the 2 outputs is - 40 µA at 3.3V / +1.6 mA at 0.4V.

4.20 CF Card Interface

The bus state controller of the SH7760 processor is able to control the processor bus in the areas 5 and 6 in compliance with PCMCIA cards. The processor does not have a complete PC card controller. This is why a PC card controller was implemented in a PLD.

The control signals of the PC card controller are routed to the J2 connector of HiCO.nect via a driver 74LVT244. This allows an easy implementation of a CF interface on an additional board.

The controller includes the 4 registers PCCISR, PCCGCR, PCCCSCR and PCCCSIER.

The following applies:

Register	Access	Value After Reset	Address	Register	Access
PCCISR	R	-	0xA4000160	8 Bits	16 Bits
PCCGCR	R/W	0x00	0xA4000162	8 Bits	16 Bits
PCCCSCR	R/W	0x00	0xA4000164	8 Bits	16 Bits
PCCCSIER	R/W	0x00	0xA4000166	8 Bits	16 Bits

The register addresses are decoded by means of the lower 11 address lines only. The registers are thus mirrored and several times available in area 1.

The data region of the PC card interface is located in area 6. The controller is able to issue level 9 interrupts.

A PCMCIA interface may only be implemented with restrictions. There is no control of address line A25, VSS and VPP, neither are the VS1 and VS2 signals analyzed. Also, the BVD1 and BVD2 signals are not analyzed. Therefore, the Battery Warning and Battery Dead states do not issue an interrupt. Although the associated enable bits have been implemented, they are of no effect here. Since neither the flash- nor I/O cards make use of the BVD signals, a CF interface may be implemented without any functional restrictions. Check for yourself if there are too many restrictions when using a PCMCIA interface. There should be no difficulties, however, in connection with Flash cards.

The controller is almost fully compatible with the PC card controller in the SH7727. For detailed information, please refer to section 30 of the SH7727 user manual.

4.21 LAN91C111 Ethernet Controller

The LAN91C111 chip from SMSC is used as Ethernet controller [2]. This controller comes with a Media Access Controller (MAC) and Physical Layer Interface (PHY) on a single chip. An on-chip SRAM serves to buffer transmit- and receive frames of 8K bytes. The chip is able to put itself to the operating modes 100 BASE-TX or 10BASE-T, both half- and full duplex.

The Ethernet controller is located in the address range 0xA4000300 through 0xA400030F. Both byte- and word accesses to the Ethernet controller are possible.

The MAC and configuration data of the Ethernet controller are stored in a 93C46 type EEPROM. The IOS lines of the controller are switched between 000 (On switch) and 111 (Off switch) using DIP switch S30 4. In this way, two different data sets may be selected in the EEPROM. By default, data set 0 is used. The DIP switch setting may be read at address 0xa40000a0 on bit 3.

The data lines as well as two status signals that serve to indicate the link status and 10/100 Mbps are connected to J3 of the HiCO.nect.

When using the Ethernet signals on an external BASE board, an appropriate 1:1 transformer is required.

4.22 Status Port, Status LEDs

An 8-bit status port is located at address 0xA40000A0; it is used to read the status of the jumper W30 the DIP switch S30 and the PLD revision code.

LED D30 may be enabled or disabled by writing to the same address via data bit 0. The following applies for the port assignment:

Address	Direction	Function	Assignment
0xA40000A0	Read	Status port	Bit [7..5] = PLD revision code Bit 4 = 0: W30 in position 1-2 1: W30 in position 2-3 Bit 3 = 0: S30-4 = On 1: S30-4 = Off Bit 2 = 0: S30-3 = On 1: S30-3 = Off Bit 1 = 0: S30-2 = On 1: S30-2 = Off Bit 0 = 0: S30-1 = On 1: S30-1 = Off
0xA40000A0	Write	Status LED	Bit[7..1] = unused Bit 0 = 0: LED = On 1: LED = Off

The DIP switches S30 actually have the following meaning:

Switch	Position	Assignment
1 - 2	on – on	Display type is TFT, 640 x 480 pixel
	on – off	Display type is TFT, 800 x 600 pixel
	off – on	Display type is SX14Q002
	off – off	Display type is ¼ VGA TFT
3	off	reserved for future use
4	off	IOS of LAN91C111, don't change

If W30 is plugged in position 1-2 after start up the Bootloader menu appears on a terminal connected to COM1. Otherwise the application is started immediately.

The second status LED D10 provides information on the current processor state by way of different brightness intensity levels. The LED cannot be controlled via software.

The following applies for the light intensity of D10:

Light Intensity D10	Processor State
Off	Reset
Dark	Sleep– or Standby mode
Bright	Normal operation

4.23 Reset

There are several ways for issuing a reset signal:

- A voltage monitor checks the supply voltages +3.3 volts and +1.5 volts and issues a reset when the respective supply voltage falls below its required level.
- Via J1 of the HiCO.nect plug connector.
- Via the JTAG interface.

- Via any write access to address 0xA4000B0.

All resets are hardware resets of the processor board issuing a hardware reset of the processor. The processor may not be "manually" reset.

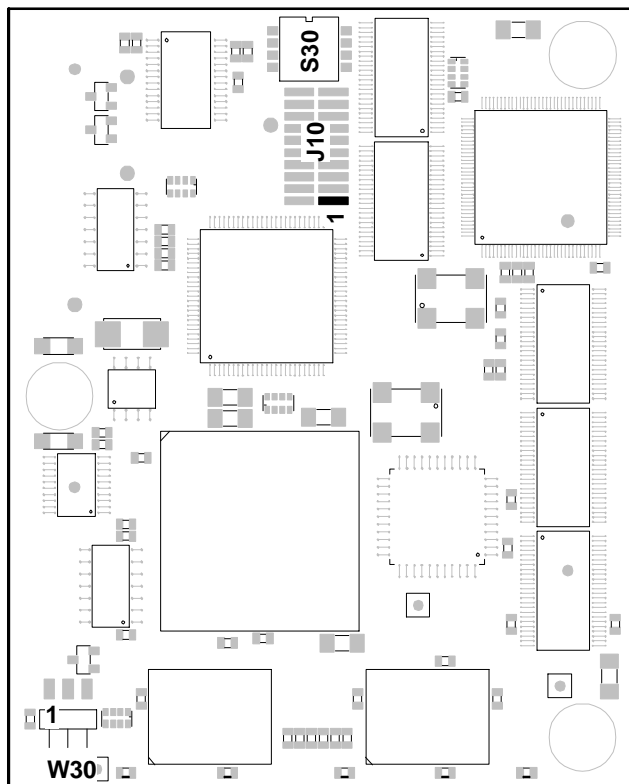
4.24 Supply Voltage

The voltage +3.3 V, +/-5%, must be fed via the HiCO.nect plug connectors. For using the USB host +5 V must be fed via J1, pin 78. This pin is only used as the voltage source for the USB supply.

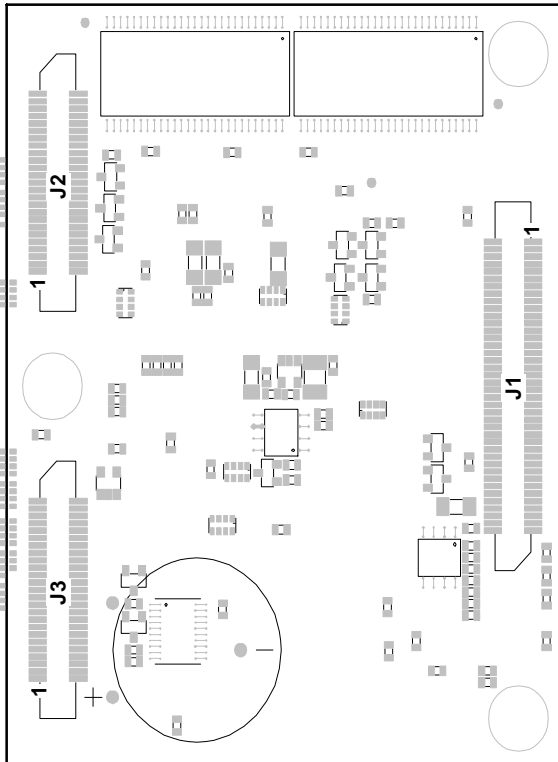
The processor core voltage 1.5V is generated on the module. It is available at connector J2, pin 35. This voltage should not be used to supply any external components. It should only be used for external monitoring the supply. The voltage is connected via a 100 Ω series resistor to protect the voltage from external shorts.

5 Location of the Connectors

Component side view:



Solder side view:



6 Pin Assignments

6.1 J1, HiCO.nect

Watch:

At the HiCO.nect interface the pin1 location of connectors J1, J2 and J3 is different compared with pin 1 marking of Hirose. For clarification both pin counts are shown here.

Type Hirose FX6-80P, 80-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	79	GND	2	80	+3.3V
3	77	ID0	4	78	ID1
5	75	ID2	6	76	n/c
7	73	A0	8	74	A1
9	71	A2	10	72	A3
11	69	A4	12	70	A5
13	67	A6	14	68	A7
15	65	A8	16	66	A9
17	63	A10	18	64	A11
19	61	A12	20	62	A13
21	59	A14	22	60	A15
23	57	A16	24	58	A17
25	55	A18	26	56	A19
27	53	A20	28	54	A21
29	51	A22	30	52	A23
31	49	A24	32	50	A25
33	47	GND	34	48	+3.3V
35	45	D0	36	46	D1
37	43	D2	38	44	D3
39	41	D4	40	42	D5

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
41	39	D6	42	40	D7
43	37	D8	44	38	D9
45	35	D10	46	36	D11
47	33	D12	48	34	D13
49	31	D14	50	32	D15
51	29	GND	52	30	+3.3V
53	27	DRQ1	54	28	CLK
55	25	DACK1#	56	26	BS#
57	23	IRQ0	58	24	RD#
59	21	IRQ1	60	22	WR#
61	19	IRQ2	62	20	WE0#
63	17	IRQ3	64	18	WE1#
65	15	NMI	66	16	WAIT#
67	13	RESO#	68	14	CS4#
69	11	RESI#	70	12	CS2#
71	9	CS0#	72	10	GND
73	7	BOOT8#	74	8	SDA5
75	5	n/c	76	6	SCL5
77	3	BAT	78	4	VCC5
79	1	GND	80	2	+3.3V

6.2 J2, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	49	ENAVEE	2	50	GND
3	47	ENAVDD	4	48	REG#
5	45	DOFF#	6	46	VS1#
7	43	M	8	44	VS2#
9	41	FLM	10	42	RDY/BSY#
11	39	CL1	12	40	CE1#
13	37	CL2	14	38	CE2#
15	35	LCD0	16	36	RESET
17	33	LCD1	18	34	PDRV#
19	31	LCD2	20	32	BVD1
21	29	LCD3	22	30	BVD2
23	27	LCD4	24	28	CD1#
25	25	LCD5	26	26	CD2#
27	23	LCD6	28	24	PWAIT#
29	21	LCD7	30	22	GND
31	19	GND	32	20	I_CE1#
33	17	CONTRAST	34	18	I_CE2#
35	15	1.5V	36	16	IOIS16#
37	13	GND	38	14	IORD#
39	11	MMC_IRQ	40	12	IOWR#
41	9	+3.3V	42	10	GND
43	7	MMC_CS#	44	8	TOUCH_X1
45	5	MMC_SCLK	46	6	TOUCH_X2
47	3	MMC_DI	48	4	TOUCH_Y1
49	1	MMC_DO	50	2	TOUCH_Y2

6.3 J3, HiCO.nect

Type Hirose FX6-50P, 50-pin

Pin HiCO.nect	Pin Hirose	Signal	Pin HiCO.nect	Pin Hirose	Signal
1	49	GPIO0/LCD8	2	50	OCO1#
3	47	GPIO1/LCD9	4	48	OCO2#
5	45	GPIO2/LCD10	6	46	CAN0_RX
7	43	GPIO3/LCD11	8	44	CAN0_TX
9	41	GPIO4/LCD12	10	42	CAN1_RX
11	39	GPIO5/LCD13	12	40	CAN1_TX
13	37	GPIO6/LCD14	14	38	CAN1_ERR
15	35	GPIO7/LCD15	16	36	TXD2
17	33	GND	18	34	RXD2
19	31	TXD1#	20	32	RTS2
21	29	RXD1#	22	30	CTS2
23	27	RTS1#	24	28	TXD3
25	25	CTS1#	26	26	RXD3
27	23	DTR1#	28	24	RTS3-CTS3
29	21	DCD1#	30	22	RTS3-CTS3
31	19	ETH_LED0#	32	20	AGND
33	17	ETH_TDP	34	18	ANI2
35	15	ETH_TDM	36	16	SS0_CK
37	13	GND	38	14	SS0_WS
39	11	ETH_RDP	40	12	SS0_DA
41	9	ETH_RDM	42	10	AC0_CLK
43	7	ETH_LED1#	44	8	n/c
45	5	USBH_5V	46	6	USBF_5V
47	3	USBH_DM	48	4	USBF_DM
49	1	USBH_DP	50	2	USBF_DP

6.4 J10, Debug Connector

Type 20-pin connector, 1.27 mm * 1.27 mm pitch

Pin	Signal	Pin	Signal
1	+3.3 V	2	+3.3 V
3	TCK	4	GND
5	TRST#	6	n/c
7	TDI	8	TDO
9	ASEBRK#	10	RESET#
11	TMS	12	HRESI#
13	PLD_TDI	14	PLD_TDO
15	PLD_TCK	16	GND
17	n/c	18	n/c
19	n/c	20	n/c

7 HiCO.nect Signal Characteristics

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	A[25 .. 0]	O	3.3	> 24	Processor address bus
J1	D[15 .. 0]	I/O	3.3	> 24	Processor data bus
J1	RD#	O	3.3	> 24	Read signal
J1	WR#	O	3.3	> 24	Write signal
J1	WE0#	O	3.3	> 24	Write enable 0 shows write access on low byte
J1	WE1#	O	3.3	> 24	Write enable 1 shows write access on high byte
J1	CLK	O	3.3	> 24	Bus clock, 64 MHz
J1	BS#	O	3.3	> 24	BS# shows the start of a bus cycle
J1	IRL[3 .. 0]	IPU 10K	3.3	-	Interrupt input code
J1	NMI	IPU 10K	3.3	-	NMI interrupt
J1	DRQ	IPU 10K	3.3	-	DMA request
J1	DACK#	O	3.3	2	DMA acknowledge
J1	RDY/WAIT#	IPU 330R	3.3	-	Ready/Wait# Input
J1	CS[4, 2, 0]#	O	3.3	2	Chip selects 4, 2, 0. Chip select 0 is for ext. boot prom
J1	RESI#	IPU 10K	3.3	-	Reset input
J1	RESO#	O	3.3	4	Reset output
J1	ID[2.. 0]	IPU	3.3	-	3-bit BASE board ID
J1	SCL5	I/O	5	-	PC bus SCL, 5 V-compatible, external pull-up 4k7 necessary

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J1	SDA5	I/O	5	10	I ² C bus SDA, 5 V-compatible, external pull-up 4k7 necessary
J1	BOOT8#	IPU 11K	3.3	-	BOOT8# switches data bus width for ext. 8-bit boot PROM
J2	ENAVEE	O	3.3	2	LCD, enable VEE
J2	ENAVDD	O	3.3	2	LCD, enable VDD
J2	M	O	3.3	2	LCD, AC or DE signal for LCD display
J2	FLM	O	3.3	2	LCD, VSYNC
J2	DOFF#	O	3.3	2	LCS, display off, 0 = off
J2	CL1	O	3.3	2	LCD, HSYNC
J2	CL2	O	3.3	2	LCD pixel clock
J2	LCD[7 .. 0]	O	3.3	2	LCD, data bits [7 .. 0]
J2	REG#	O	3.3	2	PCMCIA, REG#
J2	VS1#, VS2#	I	3.3	-	PCMCIA, VS1#, VS2#
J2	CE1#, CE2#	O	3.3	2	CE1#, CE2#, CE2#
J2	RDY/BSY#	I	3.3	-	PCMCIA, RDY/BSY#
J2	RESET	O	3.3	2	PCMCIA, RESET
J2	BVD[2 .. 1]	I	3.3	-	PCMCIA, BVD[2 .. 1]
J2	CD[2 .. 1]#	IPU 10K	3.3	-	PCMCIA, CD[2 .. 1]#
J2	WAIT	IPU 10K	3.3	-	PCMCIA, WAIT
J2	IOIS16#	I	3.3	-	PCMCIA, IOIS16#
J2	IORD#	O	3.3	2	PCMCIA, IORD#
J2	IOWR#	O	3.3	2	PCMCIA, IOWR#
J2	PDRV#	O	3.3	2	Enable for PCMCIA signal driver

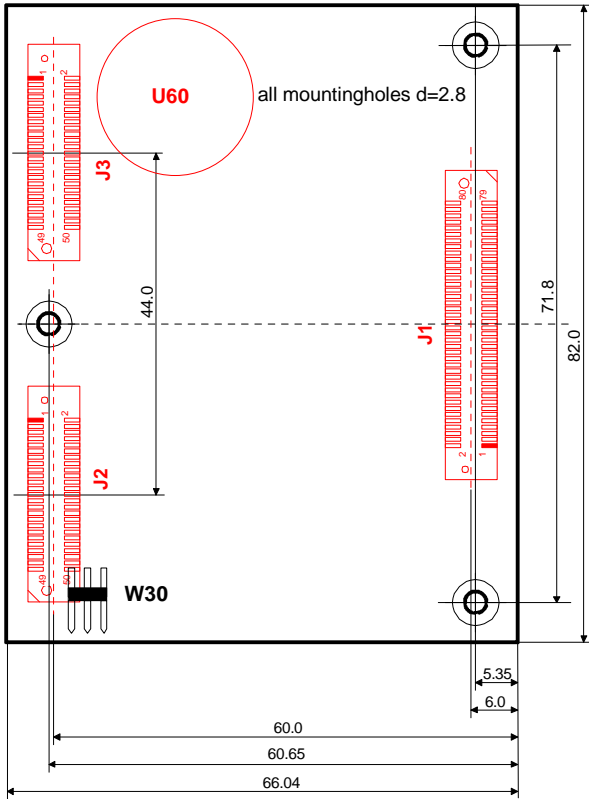
Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J2	I_CE1#	O	3.3	2	ISA Bus Interface, bus low enable
J2	I_CE2#	O	3.3	2	ISA Bus Interface, bus high enable
J2	MMC_IRQ	IPU 4K7	3.3	-	MMC, interrupt
J2	MMC_CS#	O	3.3	2	MMC, SPI mode chip select
J2	MMC_SCLK	O	3.3	2	MMC, SPI mode SCLK
J2	MMC_DO	I	3.3	-	MMC, SPI mode DO
J2	MMC_DI	O	3.3	2	MMC, SPI mode DI
J2	TOUCH_X1	A I/O	3.3	-	4-conductor touch controller, X1
J2	TOUCH_X2	A I/O	3.3	-	4-conductor touch controller, X2
J2	TOUCH_Y1	A I/O	3.3	-	4-conductor touch controller, Y1
J2	TOUCH_Y2	A I/O	3.3	-	4-conductor touch controller, Y2
J2	ANA0	AO	3.3	5	Analogue output, 0 ... +3.3 V
J3	GPIO[7 .. 0]	I/O	3.3	2	General Purpose I/O [7 .. 0], LCD[15 ... 8]
J3	TXD#	O	RS232	2	COM1, TXD
J3	RXD#	I	RS232	-	COM1, RXD
J3	RTS	O	RS232	2	COM1, RTS
J3	CTS	I	RS232	-	COM1, CTS
J3	DTR#	O	RS232	2	COM1, DTR
J3	DCD	I	RS232	-	COM1, DCD
J3	TXD2	O	3.3	2	COM2, TXD

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	RXD2	I	3.3	-	COM2, RXD
J3	RTS2	O	3.3	2	COM2, RTS
J3	CTS2	I	3.3	-	COM2, CTS
J3	TXD3	O	3.3	2	COM3, TXD
J3	RXD3	I	3.3	-	COM3, RXD
J3	RTS3	O	3.3	2	COM3, RTS
J3	CTS3	I	3.3	-	COM3, CTS
J3	OCO1#	O OC	50	220	Open Collector Out. 1
J3	OCO2#	O OC	50	220	Open Collector Out. 2
J3	CAN0_RX	I	3.3	-	CAN0 Receive
J3	CAN0_TX	O	3.3	2	CAN0 Transmit
J3	CAN1_RX	I	3.3	-	CAN1 Receive
J3	CAN1_TX	O	3.3	2	CAN1 Transmit
J3	CAN1_ERR	I	3.3	-	CAN1 Error
J3	ANI2	A I	3.3	-	Analog input ANI2
J3	SS0CK	I/O	3.3	-	IIS clock
J3	SS0WS	I/O	3.3	-	IIS word select
J3	SS0DA	I/O	3.3	-	IIS data
J3	ACCK0	I	3.3	-	Oversampling audio clock
J3	ETH_TDP	A O	-	-	Ethernet, transmit data positive
J3	ETH_TDM	A O	-	-	Ethernet, transmit data negative
J3	ETH_RDP	A I	-	-	Ethernet, receive data positive
J3	ETH_RDN	A I	-	-	Ethernet, receive data negative

Con	Name	Direction on CORE	Volt [V]	Current [mA]	Function
J3	ETH_LED0#	O	3.3	10	Ethernet, link LED
J3	ETH_LED1#	O	3.3	10	Ethernet, 10/100 Mbit LED
J3	USBF_5V	I	5	-	USB Function, Vbus recognition
J3	USBF_DP	I/O	5	-	USB Function, data positive
J3	USBF_DM	I/O	5	-	USB Function, data negative
J3	USBH_5V	O	5	500	USB Host, 5 V output
J3	USBH_DP	I/O	5	-	USB Host, data positive
J3	USBH_DM	I/O	5	-	USB Host, data negative
J1	BAT	-	3.0	10 μ A	3 V battery input
J1	VCC3	-	-	-	+ 3.3 V supply
J1	VCC5	-	-	-	+5 V supply, for USB Host
J1	GND	-	-	-	Ground

8 Dimensional Drawing

Component side view; the solder side connectors are marked red.



9 Technical Data

9.1 Mechanical Data

Weight	80 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	66 mm x 82 mm x 10 mm

9.2 Electrical Data

Supply voltage	3.3V, +/-5%
Power consumption	0.7 A max.

9.3 Environmental Conditions

Operating temperature	0 ... +70°C,
Storage temperature	-40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

10 Reference

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- [2] LAN91C111
10/100 Non-PCI Ethernet Single Chip MAC + PHY
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- [3] I²C compatible 256-Position Digital Potentiometers AD5241/5242
Datasheet
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Analog Devices Inc.

- [4] ISP1181B Full-speed Universal Serial Bus interface device
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Rev. 01 — 03 July 2002
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